SPICE Device Model SiHB10N40D



Vishay Siliconix

D Series Power MOSFET

DESCRIPTION

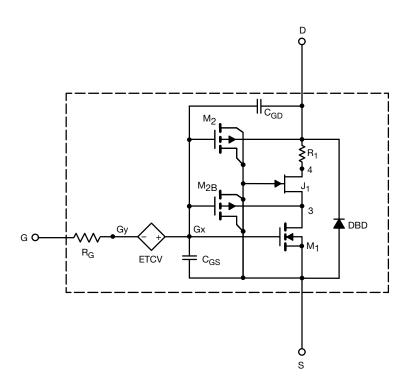
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over 25 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over 25 °C to 150 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



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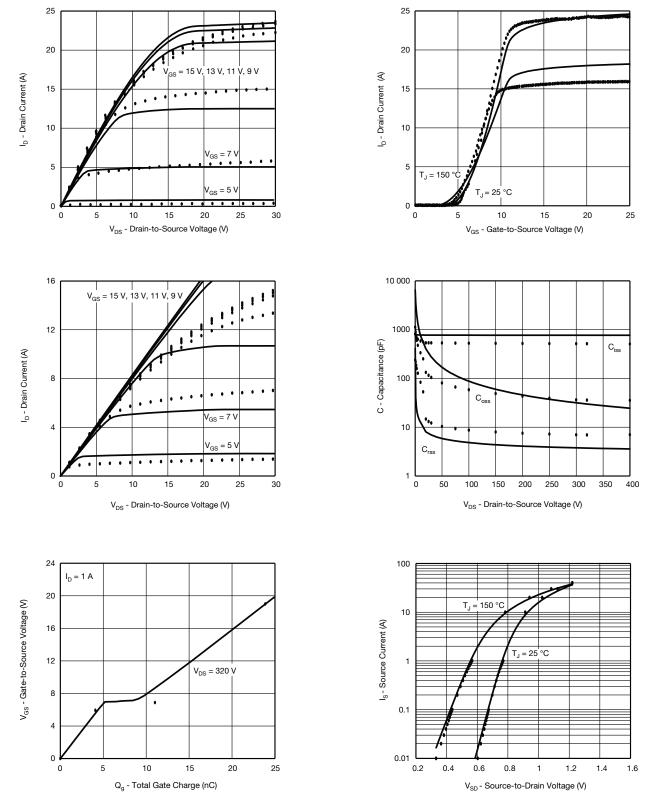
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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	4	-	V
Drain-source on-state resistance	R _{DS(on)}	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 5 \text{ A}$	0.57	0.50	Ω
Forward transconductance	9 _{fs}	$V_{DS} = 50 \text{ V}, \text{ I}_{D} = 5 \text{ A}$	2.9	2.7	S
Dynamic					
Input capacitance	C _{iss}	$V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$	770	526	pF
Output capacitance	C _{oss}		90	59	
Reverse transfer capacitance	C _{rss}		5	9	
Total gate charge	Qg	$V_{DS} = 320 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 5 \text{ A}$	13	15	nC
Gate-source charge	Q _{gs}		5	4	
Gate-drain charge	Q _{gd}		5	7	
Drain-Source Body Diode Characteris	stics				
Reverse recovery time	t _{rr}	$T_J = 25 \text{ °C}, I_F = I_S = 5 \text{ A},$ di/dt = 100 A/µs, V _R = 25 V	240	230	ns
Reverse recovery charge	Q _{rr}		1.9	1.6	μC



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COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



Note

• Dots and squares represent measured data Copyright: Vishay Intertechnology, Inc.

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3

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