

E Series Power MOSFET

DESCRIPTION

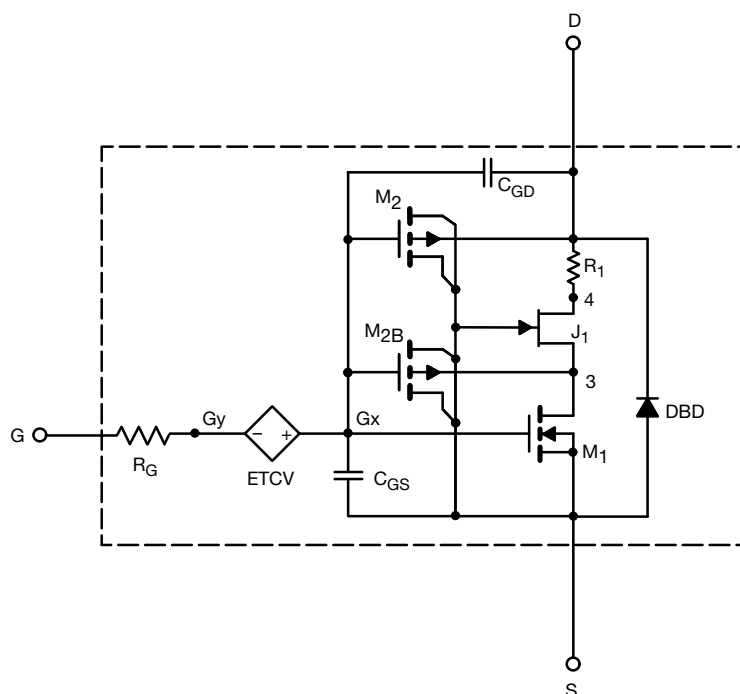
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over 25 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over 25 °C to 150 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



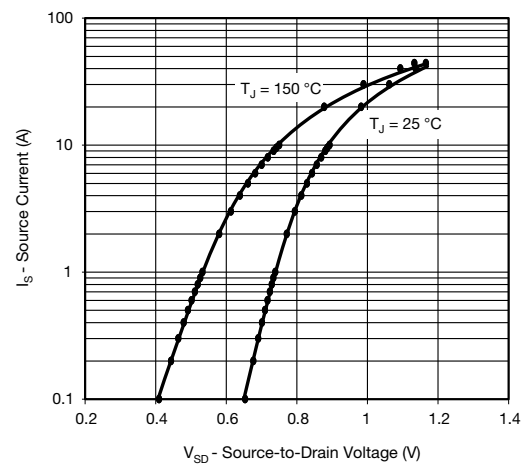
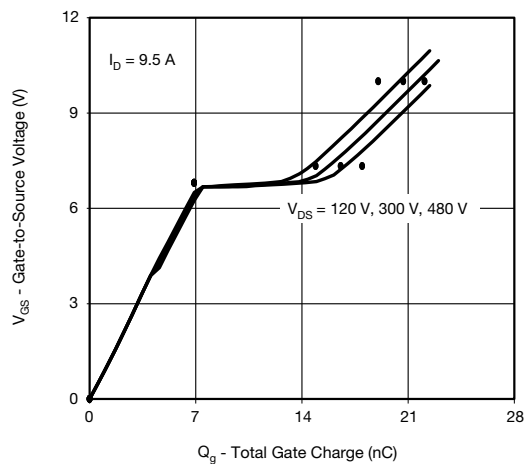
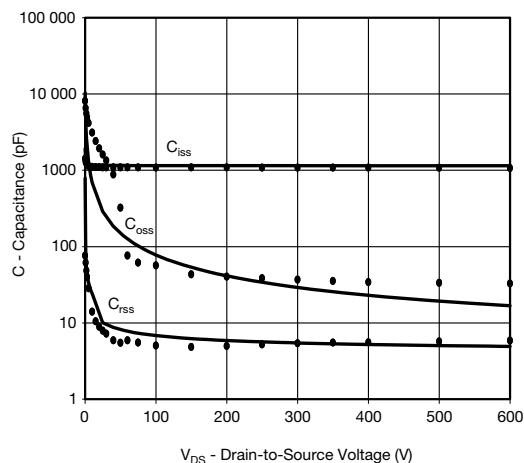
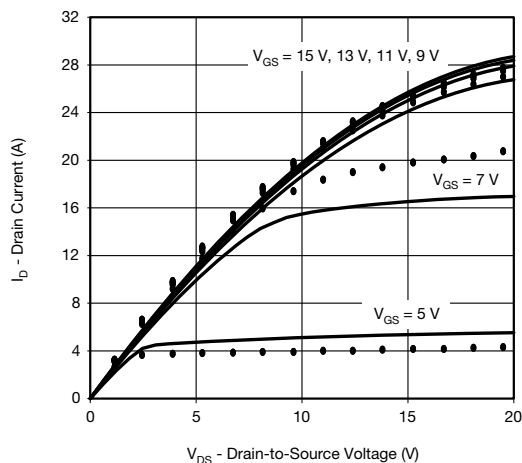
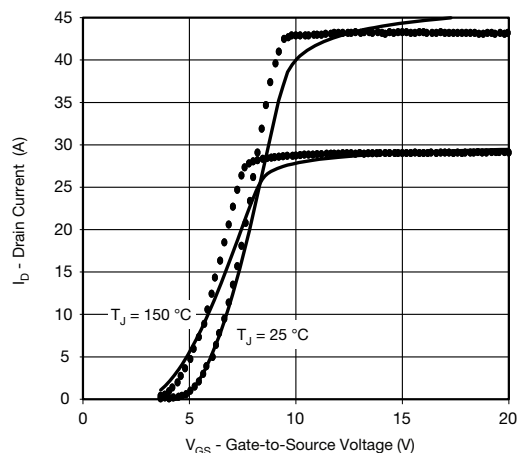
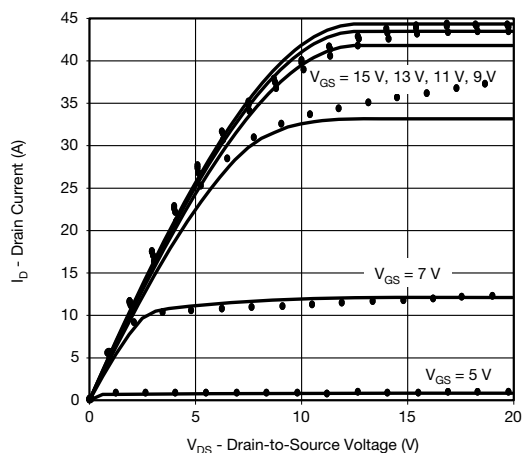
| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | |
|---|---------------------|--|----------------|---------------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | SIMULATED DATA | MEASURED DATA | UNIT |
| Static | | | | | |
| Gate-Source Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 4 | - | V |
| Drain-Source On-State Resistance ^a | R _{DS(on)} | V _{GS} = 10 V, I _D = 9.5 A | 0.193 | 0.155 | Ω |
| Forward Transconductance ^a | g _{fs} | V _{DS} = 20 V, I _D = 9.5 A | 7.6 | 5.3 | S |
| Dynamic ^b | | | | | |
| Input Capacitance | C _{iss} | V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz | 1150 | 1085 | pF |
| Output Capacitance | C _{oss} | | 73 | 56 | |
| Reverse Transfer Capacitance | C _{rss} | | 6.7 | 5 | |
| Total Gate Charge | Q _g | V _{DS} = 480 V, V _{GS} = 10 V, I _D = 9.5 A | 23 | 22 | nC |
| Gate-Source Charge | Q _{gs} | | 7 | 7 | |
| Gate-Drain Charge | Q _{gd} | | 11 | 11 | |
| Drain-Source Body Diode Characteristics | | | | | |
| Diode Forward Voltage | V _{SD} | T _J = 25 °C, I _S = 9.5 A, V _{GS} = 0 V | - | - | V |
| Reverse Recovery Time | t _{rr} | T _J = 25 °C, I _F = I _S = 9.5 A, di/dt = 100 A/μs, V _R = 25 V | 280 | 282 | ns |
| Reverse Recovery Charge | Q _{rr} | | 3.7 | 3.6 | μC |

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data

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