

## E Series Power MOSFET

### DESCRIPTION

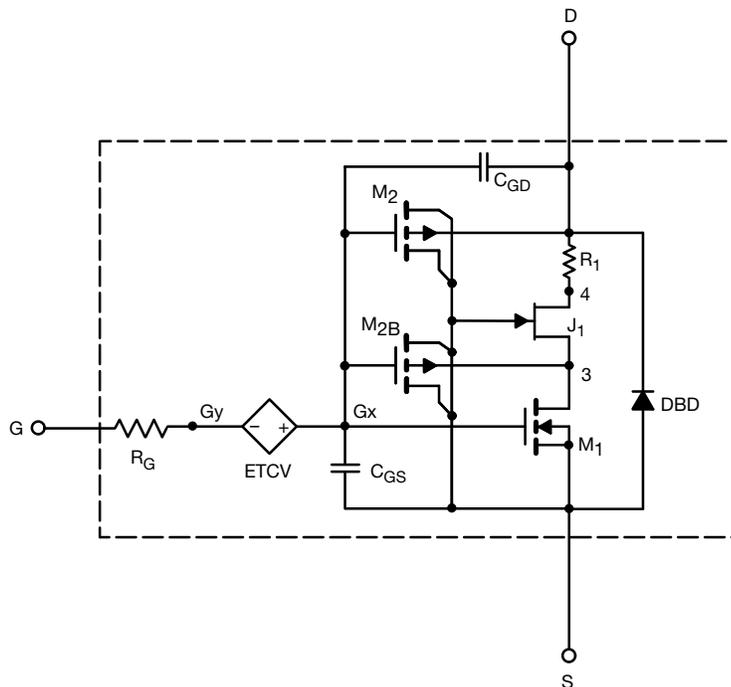
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over 25 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over 25 °C to 150 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



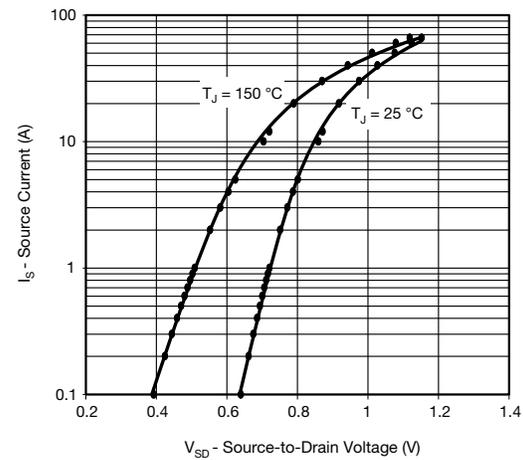
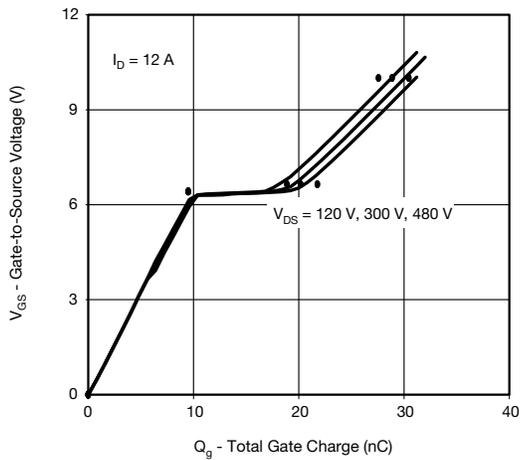
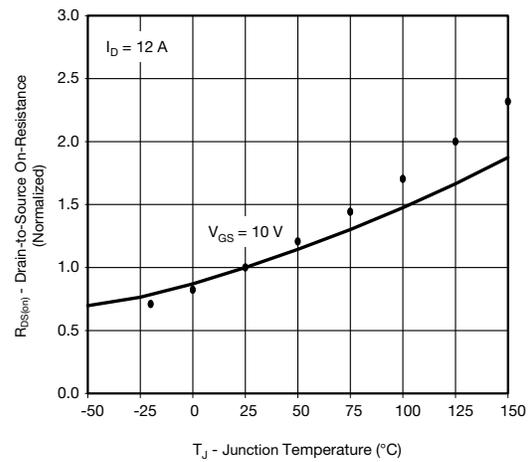
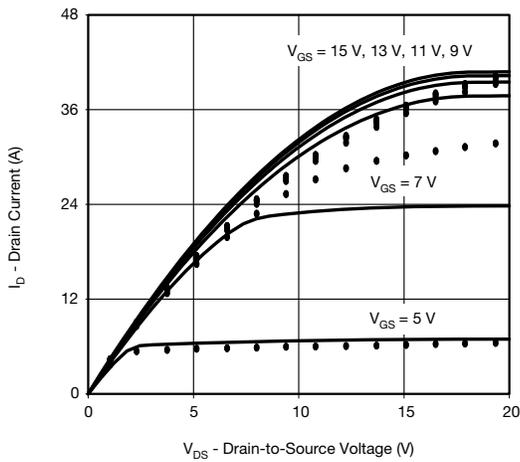
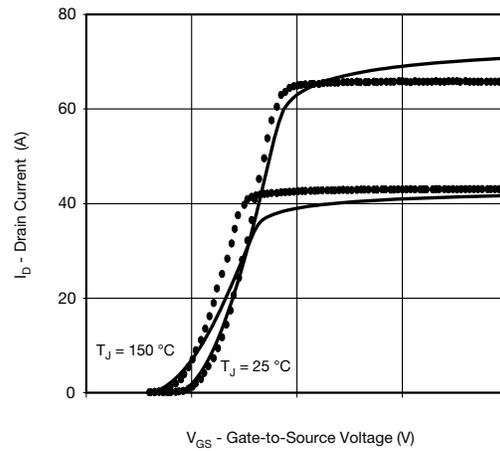
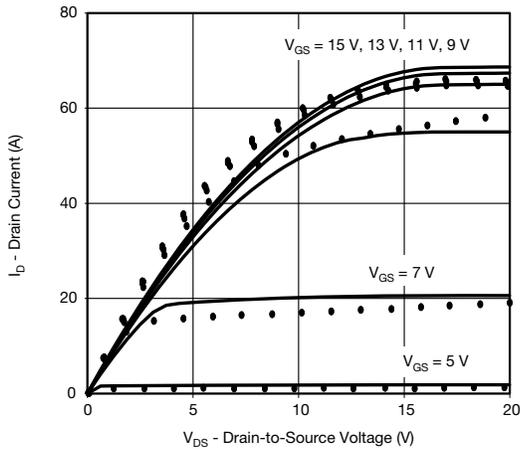
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
<b>Static</b>					
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	4	-	V
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 12\text{ A}$	0.133	0.104	$\Omega$
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 20\text{ V}$ , $I_D = 12\text{ A}$	6	6	S
<b>Dynamic <sup>b</sup></b>					
Input Capacitance	$C_{iss}$	$V_{DS} = 100\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	1700	1562	pF
Output Capacitance	$C_{oss}$		108	72	
Reverse Transfer Capacitance	$C_{rss}$		6.6	6	
Total Gate Charge	$Q_g$	$V_{DS} = 480\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 12\text{ A}$	31	30	nC
Gate-Source Charge	$Q_{gs}$		10	10	
Gate-Drain Charge	$Q_{gd}$		12	12	
<b>Drain-Source Body Diode Characteristics</b>					
Diode Forward Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 12\text{ A}$ , $V_{GS} = 0\text{ V}$	0.8	-	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = I_S = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_R = 400\text{ V}$	320	322	ns
Reverse Recovery Charge	$Q_{rr}$		4.8	4.9	$\mu\text{C}$

**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



### Note

- Dots and squares represent measured data

Copyright: Vishay Intertechnology, Inc.