SPICE Device Model SiHH120N60E



Vishay Siliconix

E Series Power MOSFET

DESCRIPTION

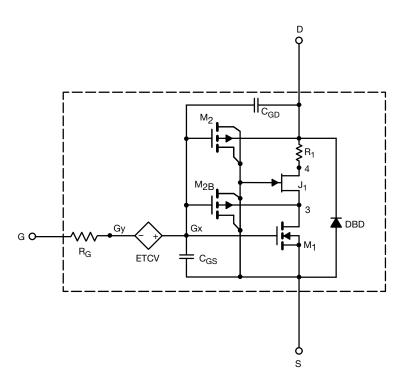
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over 25 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}\xspace$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over 25 °C to 150 °C temperature range
- · Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits

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| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | |
|--|---------------------|--|-------------------|------------------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | SIMULATED DATA | MEASURED DATA | UNIT |
| Static | | | | | |
| Gate-Source Threshold Voltage | V _{GS(th)} | $V_{DS}=V_{GS},\ I_{D}=250\ \mu A$ | 4 | - | V |
| Drain-Source On-State Resistance ^a | R _{DS(on)} | $V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$ | 0.140 | 0.106 | Ω |
| Forward Transconductance ^a | 9 _{fs} | $V_{DS} = 20 \text{ V}, \text{ I}_{D} = 12 \text{ A}$ | 10 | 6.9 | S |
| Dynamic ^b | | | | | |
| Input Capacitance | C _{iss} | $V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$ | 1600 | 1600 | pF |
| Output Capacitance | C _{oss} | | 105 | 76 | |
| Reverse Transfer Capacitance | C _{rss} | | 6 | 6 | |
| Total Gate Charge | Qg | $V_{DS} = 480 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$ | 29 | 29 | nC |
| Gate-Source Charge | Q _{gs} | | 10 | 11 | |
| Gate-Drain Charge | Q _{gd} | | 8 | 8 | |
| Drain-Source Body Diode Characteristi | cs | | | | |
| Diode Forward Voltage | V _{SD} | $T_{J} = 25 \ ^{\circ}C, I_{S} = 12 \ A, V_{GS} = 0 \ V$ | 0.9 | - | V |
| Reverse Recovery Time | t _{rr} | $T_J = 25 \text{ °C}, I_F = I_S = 12 \text{ A},$ di/dt = 100 A/µs, V _R = 400 V | 360 | 343 | ns |
| Reverse Recovery Charge | Q _{rr} | | 6 | 5.6 | μC |

Notes

a. Pulse test; pulse width $\leq 300~\mu\text{s},$ duty cycle $\leq 2~\%$

b. Guaranteed by design, not subject to production testing

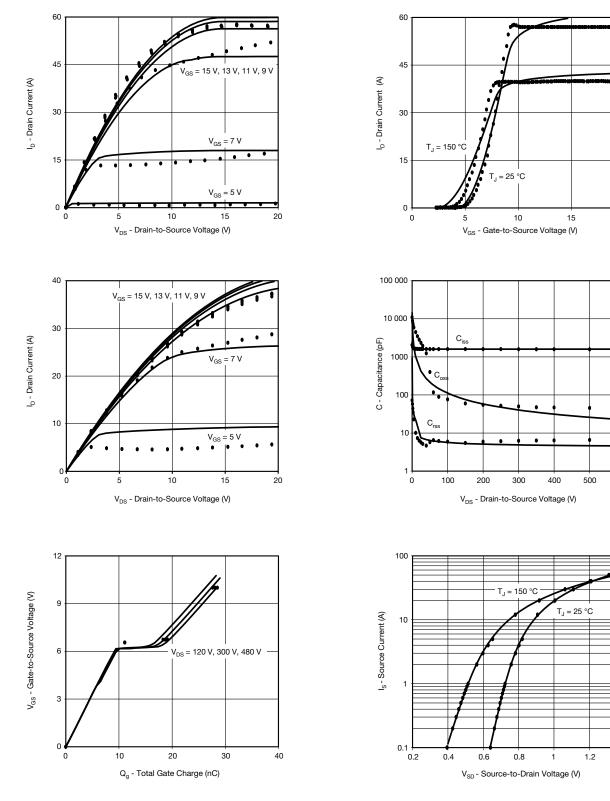


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20

600

COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



Note

• Dots and squares represent measured data Copyright: Vishay Intertechnology, Inc.

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