

## E Series Power MOSFET

### DESCRIPTION

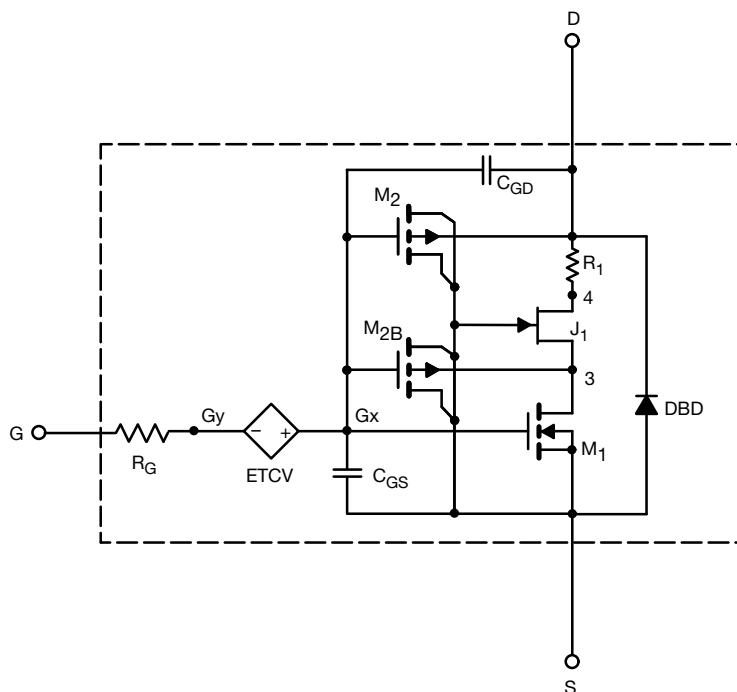
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to +150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over -55 °C to +125 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



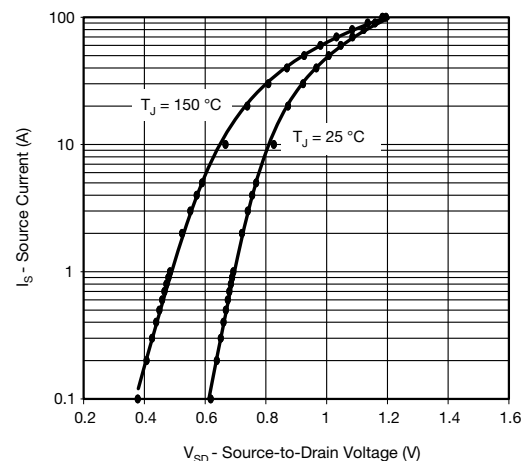
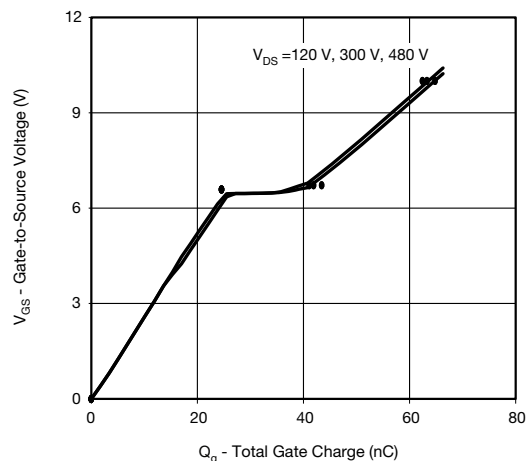
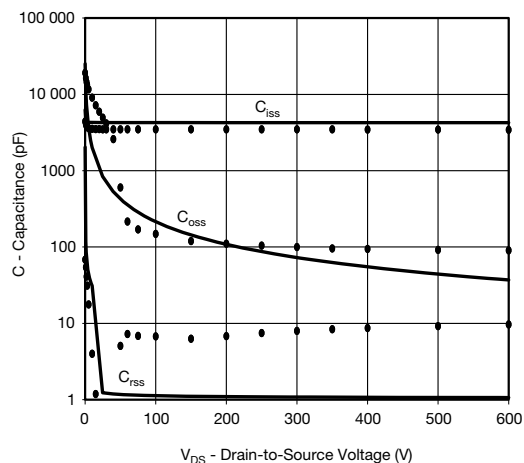
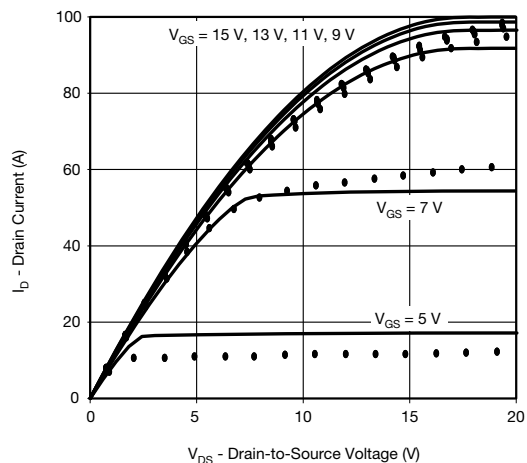
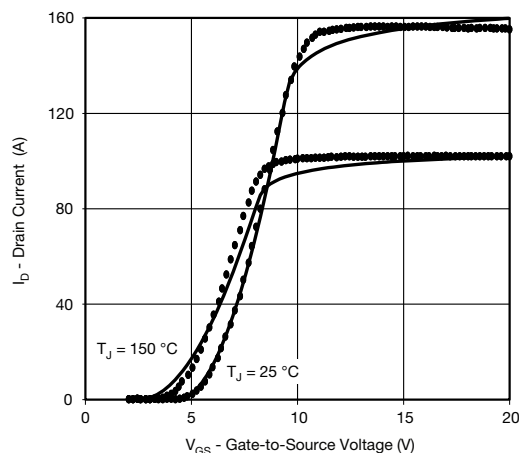
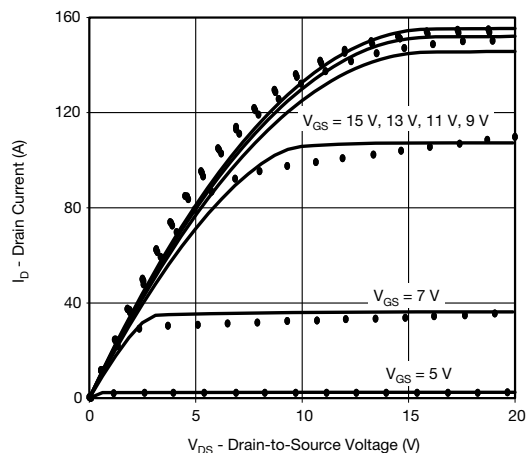
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	4	-	V
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 17 A	0.058	0.043	Ω
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 17 A	10	12	S
Dynamic <sup>b</sup>					
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, f = 1 MHz	4260	3459	pF
Output capacitance	C <sub>oss</sub>		210	148	
Reverse transfer capacitance	C <sub>rss</sub>		2	7	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 17 A	65	65	nC
Gate-source charge	Q <sub>gs</sub>		26	25	
Gate-drain charge	Q <sub>gd</sub>		17	19	
Drain-Source Body Diode Characteristics					
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 23 A, V <sub>GS</sub> = 0 V	0.9	-	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 23 A, di/dt = 100 A/μs, V <sub>R</sub> = 400 V	440	435	ns
Reverse recovery charge	Q <sub>rr</sub>		9.3	9.2	μC

**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)



### Note

- Dots and squares represent measured data

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