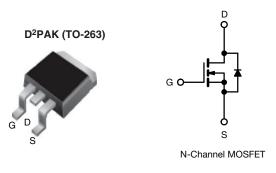
Vishay Siliconix



E Series Power MOSFET



PRODUCT SUMMARY							
V _{DS} (V) at T _J max.	650						
R _{DS(on)} typ. (Ω) at 25 °C	$V_{GS} = 10 V$	0.104					
Q _g max. (nC)	45						
Q _{gs} (nC)	10						
Q _{gd} (nC)	12						
Configuration	Single						

FEATURES

- 4th generation E series technology
- Low figure-of-merit (FOM) Ron x Qg
- Low effective capacitance (Co(er))
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
- Welding
- Induction heating
- Motor drives
- Battery chargers
- Solar (PV inverters)

ORDERING INFORMATION	
Package	D ² PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHB120N60E-GE3

ABSOLUTE MAXIMUM RATINGS (T _C	= 25 °C, unl	ess otherwis	se noted)		
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage	V _{DS}	600	v		
Gate-source voltage	V _{GS}	± 30	v		
Continuous drain surrant $(T_{1} - 150 \circ C)$	$V_{\rm ext} = 0.10$ V	T _C = 25 °C T _C = 100 °C	I _D	25	
Continuous drain current ($T_J = 150 \ ^\circ C$)	V_{GS} at 10 V	T _C = 100 °C		16	А
Pulsed drain current ^a	I _{DM}	66			
Linear derating factor			1.4	W/°C	
Single pulse avalanche energy ^b		E _{AS}	88	mJ	
Maximum power dissipation	PD	179	W		
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C
Drain-source voltage slope	T _J = 125 °C	-1 (-1)	70	1//20	
Reverse diode dv/dt d	dv/dt	50	V/ns		
Soldering recommendations (peak temperature) ^c		260	°C		

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature

b. V_{DD} = 120 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω , I_{AS} = 2.5 A

c. 1.6 mm from case

d. $I_{SD} \leq I_D$, di/dt = 100 A/µs, starting T_J = 25 °C

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COMPLIANT

HALOGEN

FREE



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THERMAL RESISTANCE RAT	INGS							
PARAMETER	SYMBOL	TYP.		MAX.		UNIT		
Maximum junction-to-ambient	R _{thJA}	-		40		°C (M)		
Maximum junction-to-case (drain)	R _{thJC}	- 0.7				- °C/W		
		•						
SPECIFICATIONS (T _J = 25 $^{\circ}$ C, u	unless otherwis	se noted)						
PARAMETER	SYMBOL	TES	T CONDIT	IONS	MIN.	TYP.	MAX.	UNIT
Static	•	•				•	•	
Drain-source breakdown voltage	V _{DS}	V _{GS} =	= 0 V, I _D = 2	250 µA	600	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I _D = 1 mA			-	0.67	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} =	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$			-	5.0	V
Gate-source leakage	I _{GSS}	\ \	$V_{\rm GS} = \pm 20$	V	-	-	± 100	nA
		Ň	/ _{GS} = ± 30	V	-	-	± 1	μA
Zous asta usltana dusia suurant		V _{DS} =	V _{DS} = 600 V, V _{GS} = 0 V			-	1	
Zero gate voltage drain current	IDSS	V _{DS} = 480 V	, V _{GS} = 0 V	′, T _J = 125 °C	-	-	10	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	١	₀ = 12 A	-	0.104	0.120	Ω
Forward transconductance a	9 _{fs}	V _{DS} :	= 20 V, I _D =	= 12 A	-	6	-	S
Dynamic							•	
Input capacitance	C _{iss}		$V_{GS} = 0 V$		-	1562	-	
Output capacitance	C _{oss}	· ·	V _{DS} = 100 °	, V,	-	72	-	
Reverse transfer capacitance	C _{rss}		f = 1 MHz		-	6	-	pF
Effective output capacitance, energy related ^a	C _{o(er)}				-	56	-	
Effective output capacitance, time related ^b	C _{o(tr)}	$V_{\rm DS} = 0.0$	/ to 480 V,	V _{GS} = 0 V	-	357	-	
Total gate charge	Qg				-	30	45	nC
Gate-source charge	Q _{gs}	V _{GS} = 10 V	I _D = 12	A, V _{DS} = 480 V	-	10	-	
Gate-drain charge	Q _{gd}				-	12	-	
Turn-on delay time	t _{d(on)}				-	19	38	
Rise time	t _r	V _{DD} =	480 V, I _D	= 12 A,	-	65	130	
Turn-off delay time	t _{d(off)}		= 10 V, R _g =		-	31	62	ns
Fall time	t _f				-	33	66	
Gate input resistance	Rg	f = 1	MHz, oper	n drain	0.3	0.65	1.3	Ω
Drain-Source Body Diode Characterist								
Continuous source-drain diode current	۱ _S	MOSFET sym showing the	bol		-	-	25	
Pulsed diode forward current	I _{SM}	integral revers p - n junction			-	-	66	A
Diode forward voltage	V _{SD}	T _J = 25 °C	C, I _S = 12 A	, V _{GS} = 0 V	-	-	1.2	V
Reverse recovery time	t _{rr}	-			- 1	322	870	ns
Reverse recovery charge	Q _{rr}	$T_J = 25$	5° C, $I_{F} = I_{S}$	= 12 A,	-	4.9	18.4	μC
Reverse recovery current	I _{RRM}	di/dt = 100 A/µs, V _R = 400 V		-	29	-	A	

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}



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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

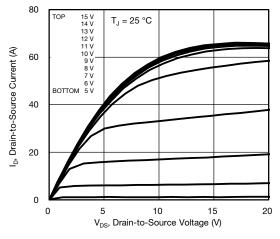


Fig. 1 - Typical Output Characteristics

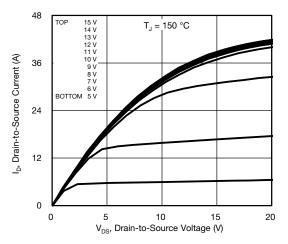


Fig. 2 - Typical Output Characteristics

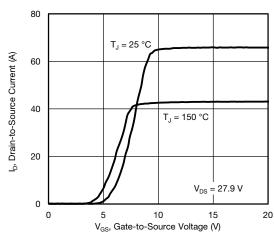


Fig. 3 - Typical Transfer Characteristics

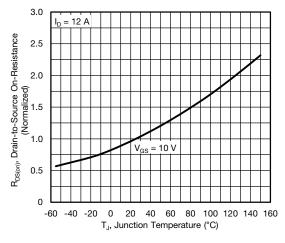


Fig. 4 - Normalized On-Resistance vs. Temperature

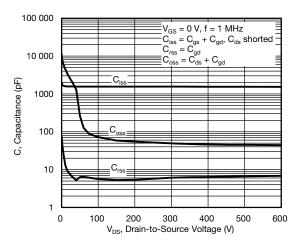


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

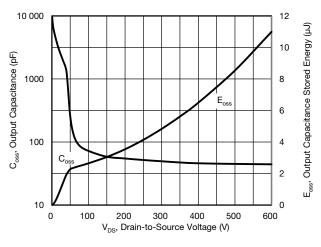


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

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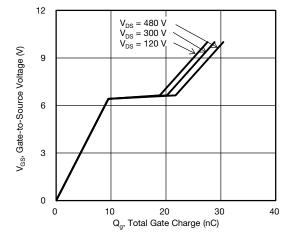


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

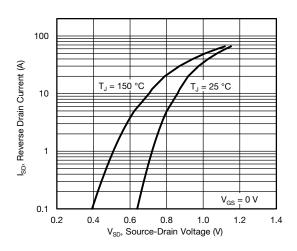


Fig. 8 - Typical Source-Drain Diode Forward Voltage

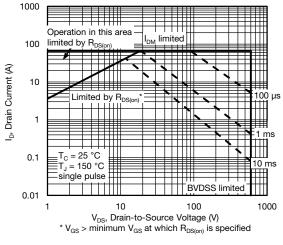


Fig. 9 - Maximum Safe Operating Area

28 24 20 I_D, Drain Current (A) 16 12 8 4 0 25 50 75 100 125 150 $T_{\rm C},$ Case Temperature (°C)

Fig. 10 - Maximum Drain Current vs. Case Temperature

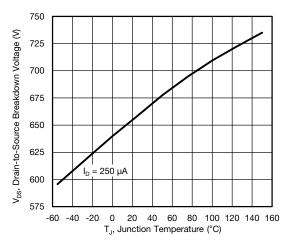


Fig. 11 - Temperature vs. Drain-to-Source Voltage

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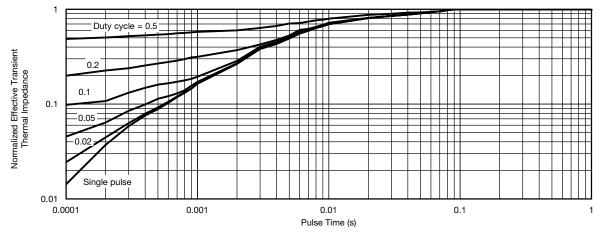


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

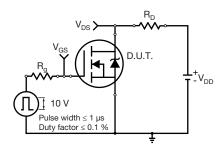


Fig. 13 - Switching Time Test Circuit

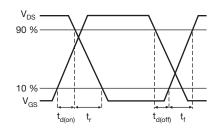


Fig. 14 - Switching Time Waveforms

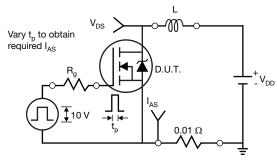


Fig. 15 - Unclamped Inductive Test Circuit

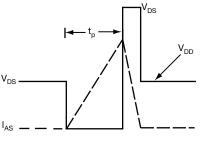


Fig. 16 - Unclamped Inductive Waveforms

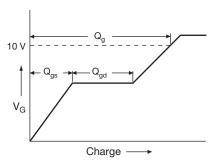


Fig. 17 - Basic Gate Charge Waveform

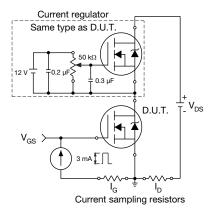


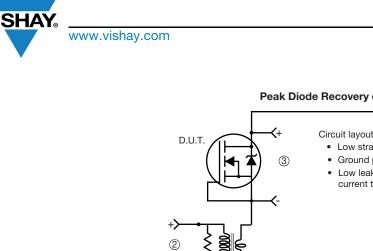
Fig. 18 - Gate Charge Test Circuit

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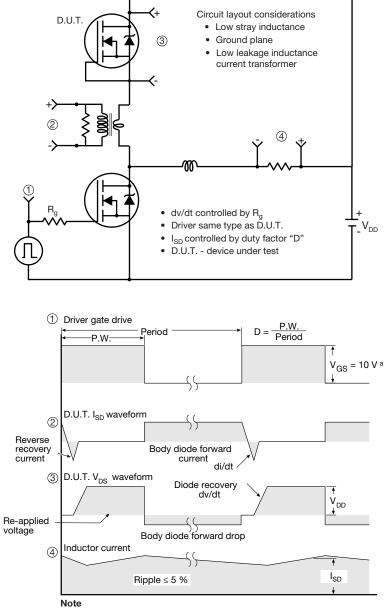
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Peak Diode Recovery dv/dt Test Circuit



a. $V_{GS} = 5$ V for logic level devices

Fig. 19 - For N-Channel

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H

A1

B

Gauge plane

L3

Detail "A" Rotated 90° CW scale 8:1

0° to 8° **Vishay Siliconix**

Seating plane

TO-263AB (HIGH VOLTAGE)

∕3 ⁄4 A

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∕₅∖

Detail A

(Datum A)

D

 $\underline{4}$ 11

	2	-	Y 2 x b2 2 x b ⊕ 0.010 @ A(■ ating 5 b1, b b1, b b1, b c) c) c) c) c) c) c) c) c) c)	$\begin{array}{c} c_{1} \\ c_{1} \\ c_{2} \\ c_{3} \\ c_{4} \\ c_{5} \\ c_{5} \\ c_{7} \\$	a - 1		Ū.	1 <u>4</u>	
	MILLIN	IETERS	INC	NCHES			MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.		DIM.	MIN.	MAX.	MIN.	MAX.
А	4.06	4.83	0.160	0.190		D1	6.86	-	0.270	-
				0.010		-		10.07	0.000	0.420
A1	0.00	0.25	0.000	0.010		E	9.65	10.67	0.380	0.120
A1 b	0.00 0.51	0.25 0.99	0.000	0.010		E1	9.65 6.22	- 10.67	0.380	-
							6.22	- 10.67 - BSC	0.245	- BSC
b	0.51	0.99	0.020	0.039		E1	6.22	-	0.245	-
b b1	0.51 0.51	0.99 0.89	0.020 0.020	0.039 0.035		E1 e	6.22 2.54	- BSC	0.245	-) BSC
b b1 b2	0.51 0.51 1.14	0.99 0.89 1.78	0.020 0.020 0.045	0.039 0.035 0.070		E1 e H	6.22 2.54 14.61	- BSC 15.88	0.245 0.100 0.575	-) BSC 0.625
b b1 b2 b3	0.51 0.51 1.14 1.14	0.99 0.89 1.78 1.73	0.020 0.020 0.045 0.045	0.039 0.035 0.070 0.068		E1 e H L	6.22 2.54 14.61 1.78	- BSC 15.88 2.79	0.245 0.100 0.575 0.070	- 0 BSC 0.625 0.110
b b1 b2 b3 c	0.51 0.51 1.14 1.14 0.38	0.99 0.89 1.78 1.73 0.74	0.020 0.020 0.045 0.045 0.015	0.039 0.035 0.070 0.068 0.029		E1 e H L L1	6.22 2.54 14.61 1.78 - -	- BSC 15.88 2.79 1.65	0.245 0.100 0.575 0.070 - -	- 0 BSC 0.625 0.110 0.066
b b1 b2 b3 c c1	0.51 0.51 1.14 1.14 0.38 0.38	0.99 0.89 1.78 1.73 0.74 0.58	0.020 0.020 0.045 0.045 0.015 0.015	0.039 0.035 0.070 0.068 0.029 0.023		E1 e H L L1 L2	6.22 2.54 14.61 1.78 - -	- BSC 15.88 2.79 1.65 1.78	0.245 0.100 0.575 0.070 - -	- 0 BSC 0.625 0.110 0.066 0.070

Α

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.

2. Dimensions are shown in millimeters (inches).

3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.

4. Thermal PAD contour optional within dimension E, L1, D1 and E1.

5. Dimension b1 and c1 apply to base metal only.

6. Datum A and B to be determined at datum plane H.

7. Outline conforms to JEDEC outline to TO-263AB.



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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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