Vishay Siliconix

E Series Power MOSFET

DESCRIPTION

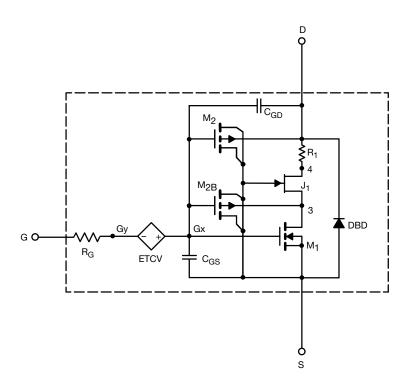
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over 25 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- · Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over 25 °C to 150 °C temperature range
- · Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits

SPICE Device Model SiHB100N60E

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	4	-	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 13 \text{ A}$	0.115	0.086	Ω
Forward Transconductance ^a	9 _{fs}	V _{DS} = 8 V, I _D = 13 A	13	11	S
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	2160	1851	pF
Output Capacitance	C _{oss}		134	84	
Reverse Transfer Capacitance	C _{rss}		6	5	
Total Gate Charge	Qg	$V_{DS} = 480 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 13 \text{ A}$	33	33	nC
Gate-Source Charge	Q_{gs}		13	13	
Gate-Drain Charge	Q_{gd}		10	10	
Drain-Source Body Diode Characteristics					
Diode Forward Voltage	V_{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 13 \text{A}, V_{GS} = 0 \text{V}$	0.9	-	V
Reverse Recovery Time	t _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = I_S = 13 \text{A},$ $di/dt = 100 \text{A/}\mu\text{s}, V_R = 25 \text{V}$	360	358	ns
Reverse Recovery Charge	Q _{rr}		6.3	5.1	μC

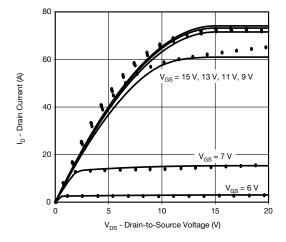
Notes

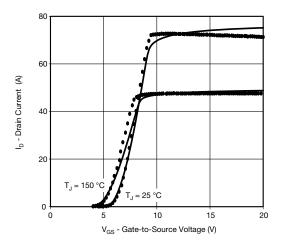
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing

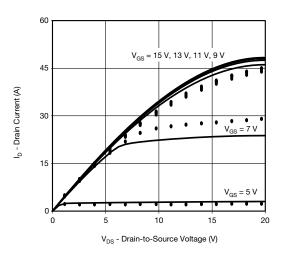
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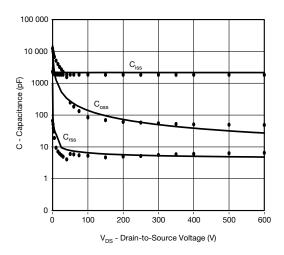
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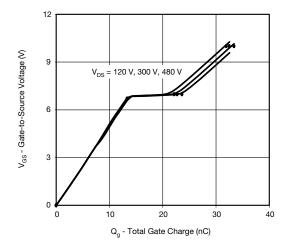
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25~^{\circ}\text{C}$, unless otherwise noted)

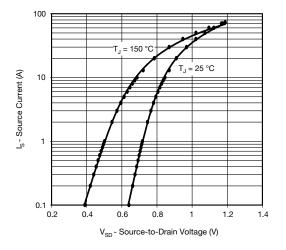












Note

· Dots and squares represent measured data Copyright: Vishay Intertechnology, Inc.



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