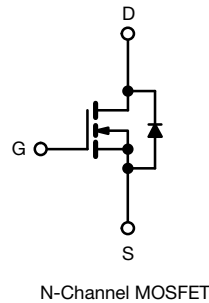
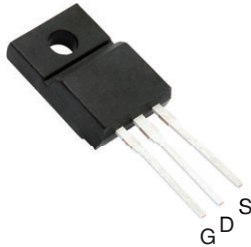


EF Series Power MOSFET With Fast Body Diode

TO-220 FULLPAK


FEATURES

- 4th generation E series technology
- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low effective capacitance ($C_{o(er)}$)
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V	0.059
Q_g max. (nC)	77	
Q_{gs} (nC)	19	
Q_{gd} (nC)	16	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free and halogen-free	SiHF068N60EF-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	600	V
Gate-source voltage	V_{GS}	± 30	
Continuous drain current ($T_J = 150$ °C) ^e	V_{GS} at 10 V	$T_C = 25$ °C	16
		$T_C = 100$ °C	10
Pulsed drain current ^a	I_{DM}	115	A
Linear derating factor		0.31	
Single pulse avalanche energy ^b	E_{AS}	226	mJ
Maximum power dissipation	P_D	39	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	dV/dt	100	V/ns
Reverse diode dV/dt ^d			
Soldering recommendations (peak temperature) ^c	For 10 s	260	°C
Mounting torque, M3 screw		0.6	Nm

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 120$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 4$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $di/dt = 210$ A/ μ s, starting $T_J = 25$ °C
- Limited by maximum junction temperature



THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Maximum junction-to-ambient	R _{thJA}	65	°C/W
Maximum junction-to-case (drain)	R _{thJC}	3.2	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	600	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA	-	0.63	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	3	-	5	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V	-	-	± 100	nA
		V _{GS} = ± 30 V	-	-	± 1	μA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 480 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C	-	-	2	mA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V I _D = 16 A	-	0.059	0.068	Ω
Forward transconductance	g _{fs}	V _{DS} = 30 V, I _D = 16 A	-	9	-	S
Dynamic						
Input capacitance	C _{iSS}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz	-	2628	-	pF
Output capacitance	C _{oss}		-	122	-	
Reverse transfer capacitance	C _{rSS}		-	7	-	
Effective output capacitance, energy related ^a	C _{o(er)}		-	87	-	
Effective output capacitance, time related ^b	C _{o(tr)}	V _{DS} = 0 V to 480 V, V _{GS} = 0 V	-	543	-	
Total gate charge	Q _g	V _{GS} = 10 V I _D = 16 A, V _{DS} = 480 V	-	51	77	nC
Gate-source charge	Q _{gs}		-	19	-	
Gate-drain charge	Q _{gd}		-	16	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 480 V, I _D = 16 A, V _{GS} = 10 V, R _g = 9.1 Ω	-	27	54	ns
Rise time	t _r		-	55	83	
Turn-off delay time	t _{d(off)}		-	53	80	
Fall time	t _f		-	35	70	
Gate input resistance	R _g		f = 1 MHz, open drain	0.3	0.7	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	41	A
Pulsed diode forward current	I _{SM}		-	-	115	
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 16 A, V _{GS} = 0 V	-	-	1.2	V
Reverse recovery time	t _{rr}	T _J = 25 °C, I _F = I _S = 16 A, di/dt = 100 A/μs, V _R = 400 V	-	152	304	ns
Reverse recovery charge	Q _{rr}		-	1	2	μC
Reverse recovery current	I _{RRM}		-	14	-	A

Notes

- a. C_{oss(er)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
- b. C_{oss(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

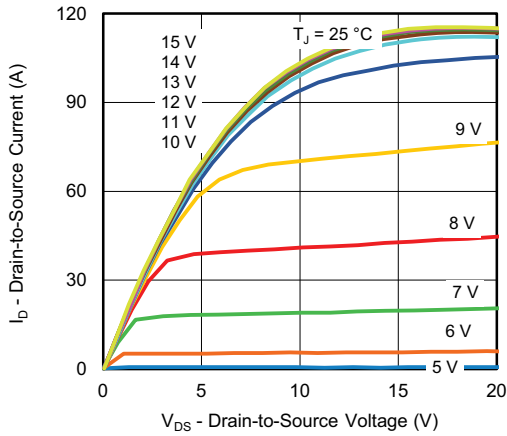


Fig. 1 - Typical Output Characteristics

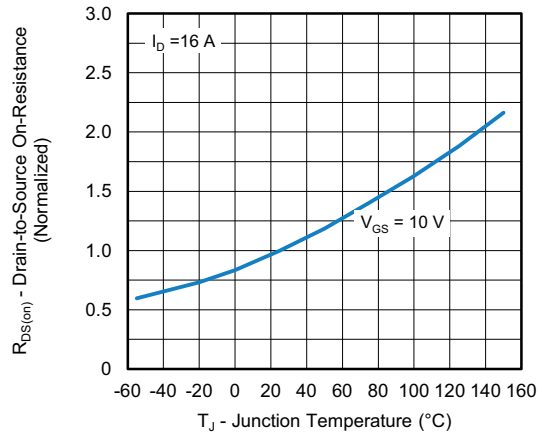


Fig. 4 - Normalized On-Resistance vs. Temperature

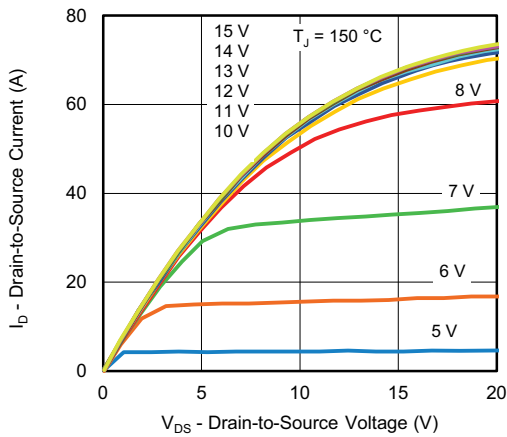


Fig. 2 - Typical Output Characteristics

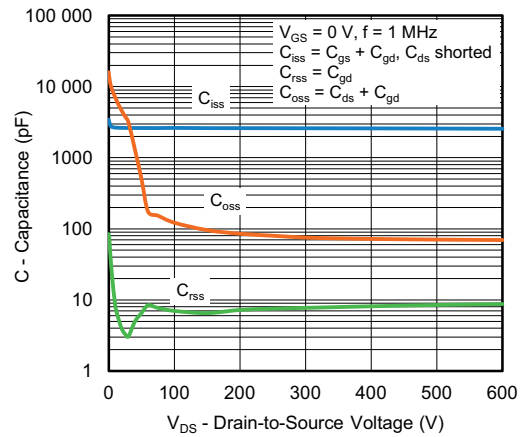


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

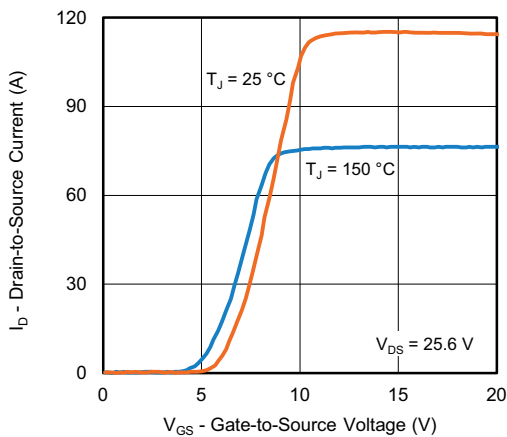


Fig. 3 - Typical Transfer Characteristics

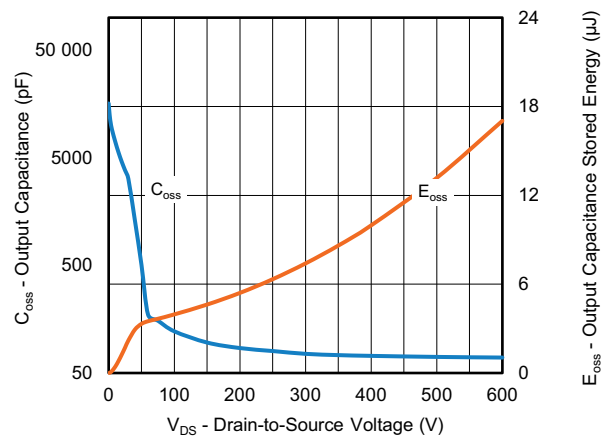


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

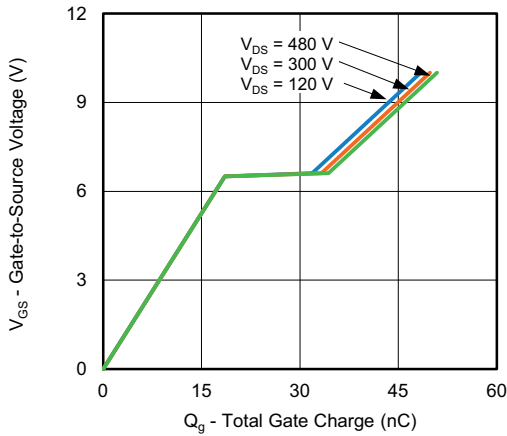


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

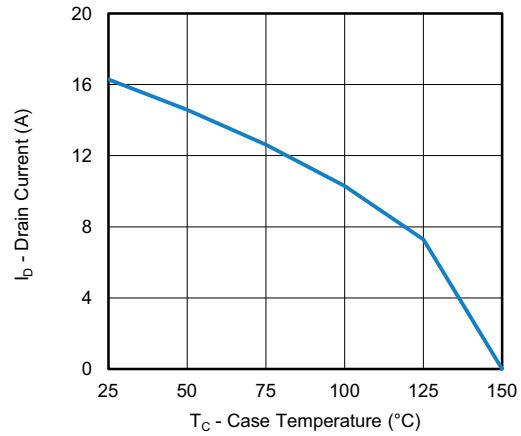


Fig. 10 - Maximum Drain Current vs. Case Temperature

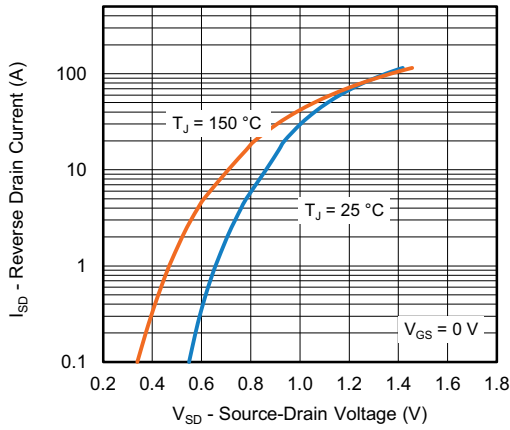


Fig. 8 - Typical Source-Drain Diode Forward Voltage

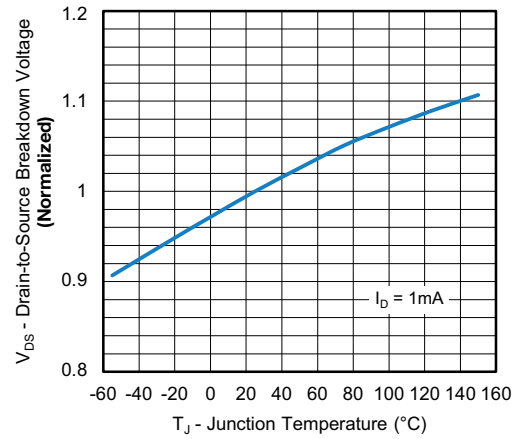


Fig. 11 - Temperature vs. Drain-to-Source Voltage

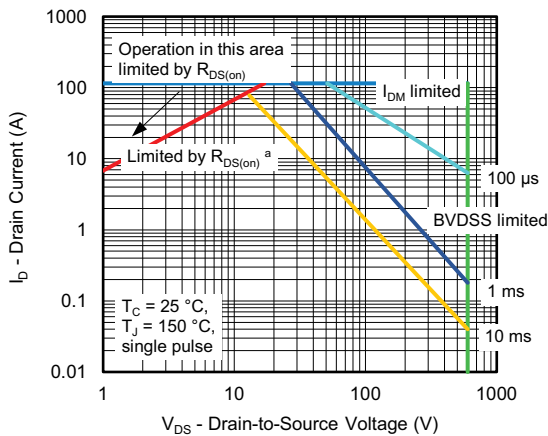


Fig. 9 - Maximum Safe Operating Area

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

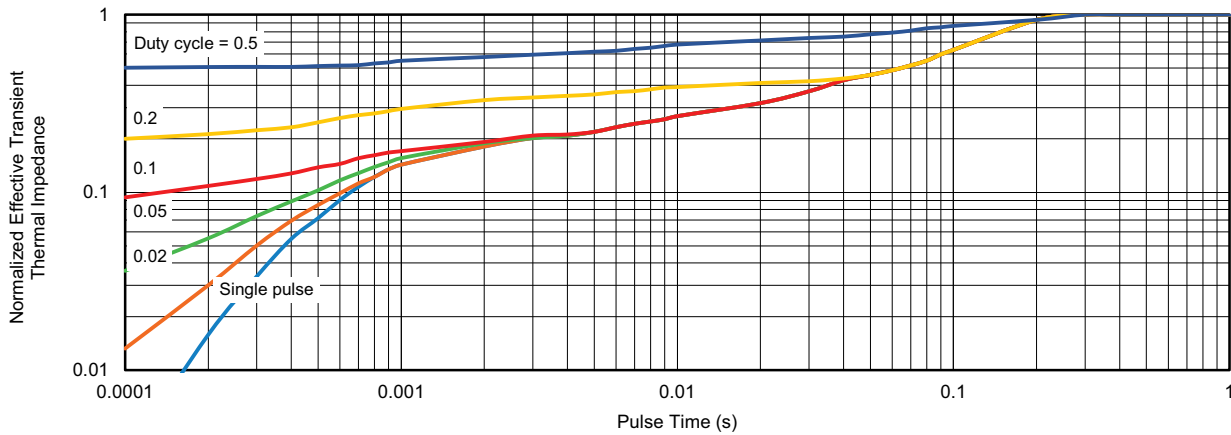


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

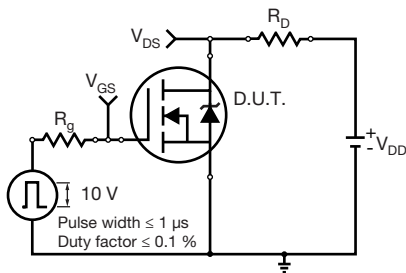


Fig. 13 - Switching Time Test Circuit

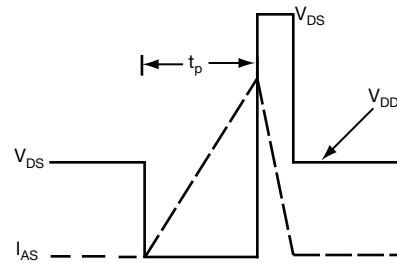


Fig. 16 - Unclamped Inductive Waveforms

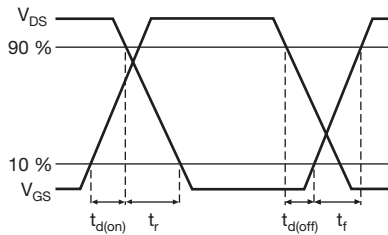


Fig. 14 - Switching Time Waveforms

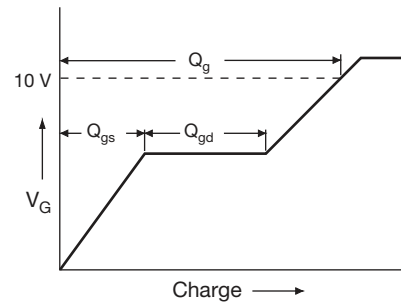


Fig. 17 - Basic Gate Charge Waveform

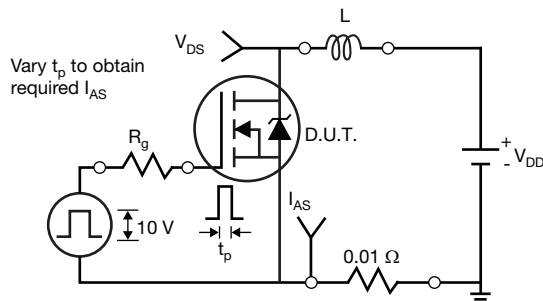


Fig. 15 - Unclamped Inductive Test Circuit

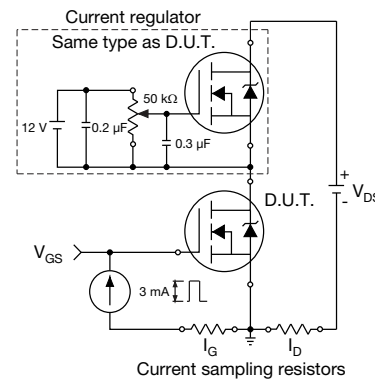


Fig. 18 - Gate Charge Test Circuit



Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

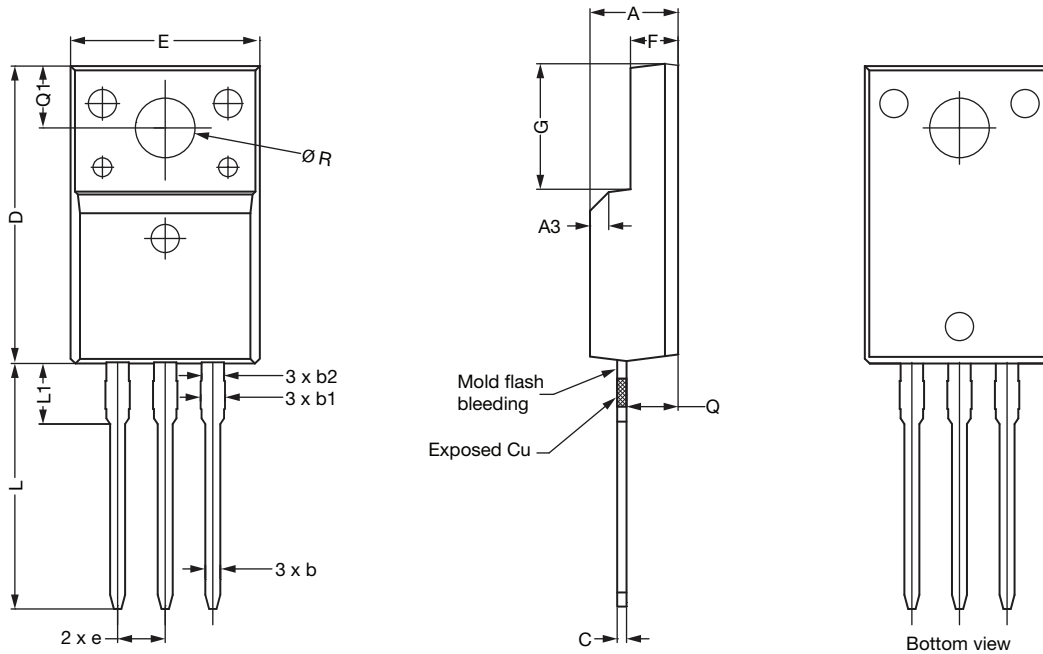
Fig. 19 - For N-Channel

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TO-220 FULLPAK (High Voltage)

OPTION 1: FACILITY CODE = 9



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
$\varnothing R$	3.08	3.18	3.28

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking



OPTION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

ECN: E19-0180-Rev. D, 08-Apr-2019
DWG: 5972

Notes

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2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking



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