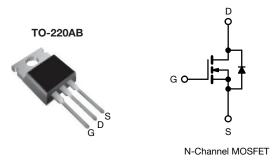
SiHP15N80AE

Vishay Siliconix



E Series Power MOSFET



PRODUCT SUMMARY				
V _{DS} (V) at T _J max.	850			
R _{DS(on)} typ. (Ω) at 25 °C	$V_{GS} = 10 \text{ V}$	0.304		
Q _g max. (nC)	53			
Q _{gs} (nC)	8			
Q _{gd} (nC)	16			
Configuration	Single			

FEATURES

- Low figure-of-merit (FOM) Ron x Qg
- Low effective capacitance (C_{o(er)})
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free and halogen-free	SiHP15N80AE-GE3

PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage	V _{DS}	800	v		
Gate-source voltage	V _{GS}	± 30	v		
Continuous drain surront $(T = 150 ^{\circ}\text{C})$	at 10 V $\frac{T_{C} = 25 \text{ °C}}{T_{C} = 100 \text{ °C}}$	- I _D -	13		
Continuous drain current ($T_J = 150 \text{ °C}$) V_{GS} a	$T_{\rm C} = 100 ^{\circ}{\rm C}$		8	А	
Pulsed drain current ^a	I _{DM}	29			
Linear derating factor			1.25	W/°C	
Single pulse avalanche energy ^b		E _{AS}	28	mJ	
Maximum power dissipation	PD	156	W		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C	
Drain-source voltage slope	T _J = 125 °C	dv/dt 100			
Reverse diode dv/dt ^d	se diode dv/dt ^d		14	V/ns	
Soldering recommendations (peak temperature) c	For 10 s		260	°C	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature

b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω , I_{AS} = 1.4 A

c. 1.6 mm from case

d. $I_{SD} \leq I_D$, di/dt = 100 A/µs, starting T_J = 25 °C





PARAMETER	SYMBOL	TYP.		MAX.		UNIT		
Maximum junction-to-ambient	R _{thJA}	-		62				
Maximum junction-to-case (drain)	R _{thJC}	-		0.8		- °C/W		
	•							
SPECIFICATIONS (T _J = 25 °C,	unless otherw	ise noted)						
PARAMETER	SYMBOL			ONS	MIN.	TYP.	MAX.	UNI
Static							L	<u> </u>
Drain-source breakdown voltage	V _{DS}	V _{GS} =	= 0 V, I _D = 25	50 μA	800	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I	_D = 1 mA	-	0.8	-	V/°(
Gate-source threshold voltage (N)	V _{GS(th)}		$V_{DS} = V_{GS}, I_D = 250 \ \mu A$		2	-	4	V
		,	$V_{GS} = \pm 20 V$ $V_{GS} = \pm 30 V$		-	-	± 100	nA
Gate-source leakage	I _{GSS}				-	-	± 1	μA
	,		= 800 V, V _{GS}		-	-	1	
Zero gate voltage drain current	IDSS	V _{DS} = 640 V	$V_{DS} = 640 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125 \text{ °C}$		-	-	10	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I	= 7.5 A	-	0.304	0.350	Ω
Forward transconductance ^a	9 _{fs}	V _{DS} :	= 10 V, I _D =	7.5 A	-	5.9	-	S
Dynamic					•	•		
Input capacitance	C _{iss}	$V_{GS} = 0 V,$ $V_{DS} = 100 V,$ f = 1 MHz $V_{DS} = 0 V \text{ to } 480 V, V_{GS} = 0 V$		-	1093	-	pF	
Output capacitance	C _{oss}			-	49	-		
Reverse transfer capacitance	C _{rss}			-	5	-		
Effective output capacitance, energy related	C _{o(er)}			-	35	-		
Effective output capacitance, time related	C _{o(tr)}			-	212	-		
Total gate charge	Qg	V _{GS} = 10 V I _D = 7.5 A, V _{DS} = 640 V		-	35	53	nC	
Gate-source charge	Q _{gs}			-	8	-		
Gate-drain charge	Q _{gd}				-	16	-	1
Turn-on delay time	t _{d(on)}	V_{DD} = 640 V, I _D = 7.5 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	15	30	- ns	
Rise time	t _r			-	22	44		
Turn-off delay time	t _{d(off)}			-	35	70		
Fall time	t _f			-	30	60		
Gate input resistance	R _g	f = 1 MHz, open drain		0.2	0.5	1.1	Ω	
Drain-Source Body Diode Characteris								
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	13	A	
Pulsed diode forward current	I _{SM}			-	-	29		
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 7.5 A, V _{GS} = 0 V		-	-	1.2	V	
Reverse recovery time	t _{rr}	$T_{\rm J} = 25 ^{\circ}\text{C}, I_{\rm F} = I_{\rm S} = 7.5 \text{A}, \\ \text{di/dt} = 100 \text{A/}\mu\text{s}, \text{V}_{\rm R} = 25 \text{V}$		-	333	666	ns	
Reverse recovery charge	Q _{rr}			-	3.7	7.4	μ	
Reverse recovery current	I _{RRM}			-	19	-	Α	



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

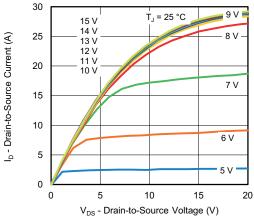


Fig. 1 - Typical Output Characteristics

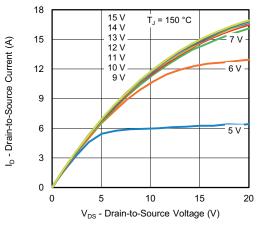


Fig. 2 - Typical Output Characteristics

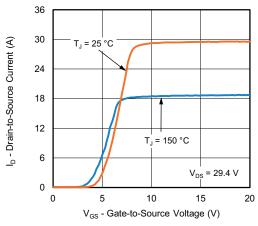


Fig. 3 - Typical Transfer Characteristics

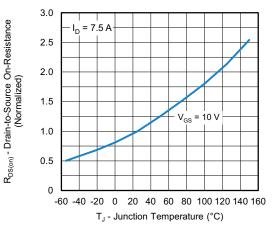


Fig. 4 - Normalized On-Resistance vs. Temperature

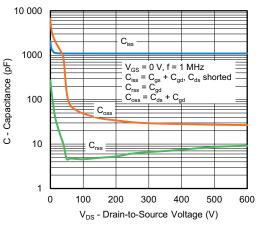
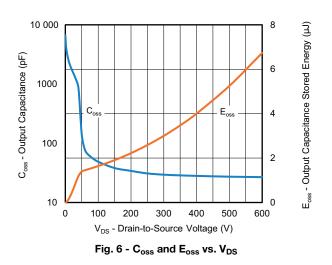


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



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3 For technical questions, contact: <u>hvm@vishay.com</u> Document Number: 92351

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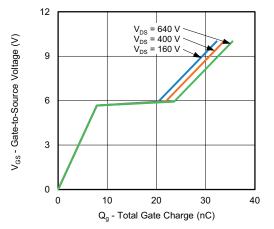


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

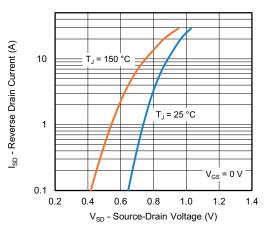


Fig. 8 - Typical Source-Drain Diode Forward Voltage

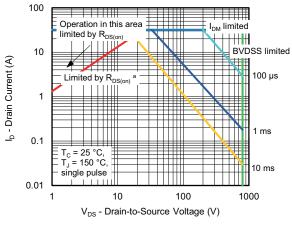
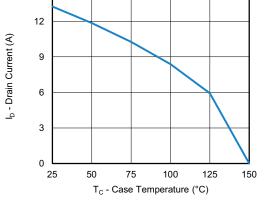


Fig. 9 - Maximum Safe Operating Area

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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Fig. 10 - Maximum Drain Current vs. Case Temperature

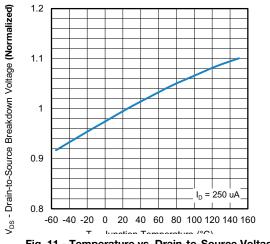


Fig. 11 - Temperature vs. Drain-to-Source Voltage

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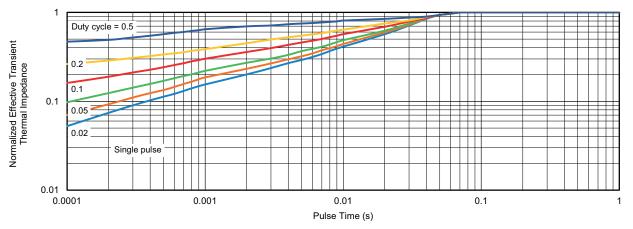


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

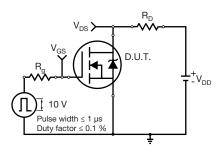


Fig. 13 - Switching Time Test Circuit

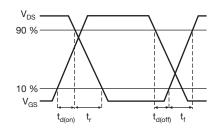


Fig. 14 - Switching Time Waveforms

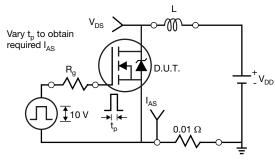


Fig. 15 - Unclamped Inductive Test Circuit

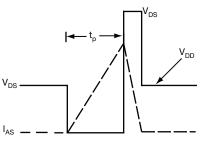


Fig. 16 - Unclamped Inductive Waveforms

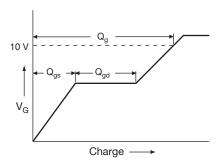


Fig. 17 - Basic Gate Charge Waveform

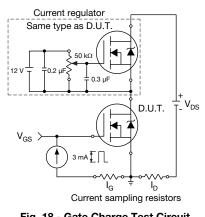


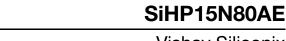
Fig. 18 - Gate Charge Test Circuit

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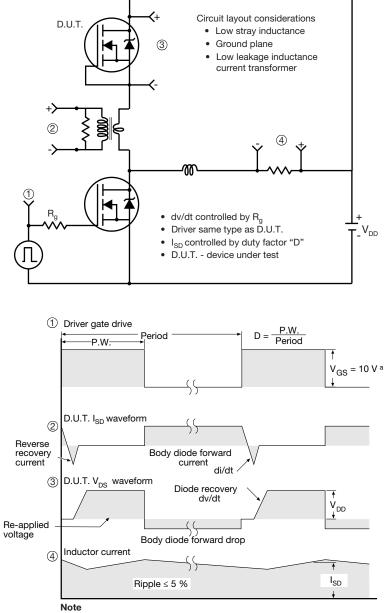
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Peak Diode Recovery dv/dt Test Circuit



a. $V_{GS} = 5$ V for logic level devices

Fig. 19 - For N-Channel

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