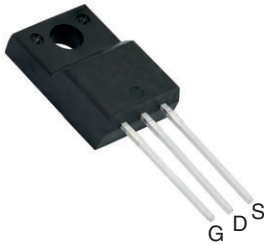


E Series Power MOSFET

Thin-Lead TO-220 FULLPAK


N-Channel MOSFET

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low effective capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Integrated Zener diode ESD protection
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


ROHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	850	
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V	1.17
Q_g max. (nC)	16.5	
Q_{gs} (nC)	3	
Q_{gd} (nC)	6	
Configuration	Single	

ORDERING INFORMATION

Package	Thin-Lead TO-220 FULLPAK
Lead (Pb)-free and halogen-free	SiHA5N80AE-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	800	V
Gate-source voltage	V_{GS}	± 30	
Continuous drain current ($T_J = 150$ °C) ^e	V_{GS} at 10 V	$T_C = 25$ °C	3.0
		$T_C = 100$ °C	1.9
Pulsed drain current ^a	I_{DM}	7	A
Linear derating factor		0.5	W/°C
Single pulse avalanche energy ^b	E_{AS}	17	mJ
Maximum power dissipation	P_D	29	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	dv/dt	$T_J = 125$ °C	70
Reverse diode dv/dt ^d		0.3	
Soldering recommendations (peak temperature) ^c	For 10 s	260	°C
Mounting torque, M3 screw		0.6	Nm

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 1.1$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $di/dt = 100$ A/ μ s, starting $T_J = 25$ °C
- Limited by maximum junction temperature



THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	65	°C/W
Maximum junction-to-case (drain)	R _{thJC}	4.3	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	800	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA	-	0.8	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	-	4	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V	-	-	± 10	μA
		V _{GS} = ± 30 V	-	-	± 50	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 800 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 640 V, V _{GS} = 0 V, T _J = 125 °C	-	-	10	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 1.5 A	-	1.17	1.35	Ω
Forward transconductance ^a	g _{fs}	V _{DS} = 30 V, I _D = 2 A	-	1.2	-	S
Dynamic						
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz	-	321	-	pF
Output capacitance	C _{oss}		-	20	-	
Reverse transfer capacitance	C _{rss}		-	4	-	
Effective output capacitance, energy related ^a	C _{o(er)}	V _{DS} = 0 V to 480 V, V _{GS} = 0 V	-	14	-	pF
Effective output capacitance, time related ^b	C _{o(tr)}		-	71	-	
Total gate charge	Q _g	V _{GS} = 10 V, I _D = 2 A, V _{DS} = 640 V	-	11	16.5	nC
Gate-source charge	Q _{gs}		-	3	-	
Gate-drain charge	Q _{gd}		-	6	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 640 V, I _D = 2 A, V _{GS} = 10 V, R _g = 9.1 Ω	-	12	24	ns
Rise time	t _r		-	8	16	
Turn-off delay time	t _{d(off)}		-	10	20	
Fall time	t _f		-	28	56	
Gate input resistance	R _g		f = 1 MHz, open drain	1.6	3.2	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	4.4	A
Pulsed diode forward current	I _{SM}		-	-	7	
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 2 A, V _{GS} = 0 V	-	-	1.2	V
Reverse recovery time	t _{rr}	T _J = 25 °C, I _F = I _S = 2 A, di/dt = 100 A/μs, V _R = 25 V	-	267	534	ns
Reverse recovery charge	Q _{rr}		-	1.2	2.4	μC
Reverse recovery current	I _{RRM}		-	7.5	-	A

Notes

- a. C_{oss(er)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 V to 480 V V_{DSS}
- b. C_{oss(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to 480 V V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

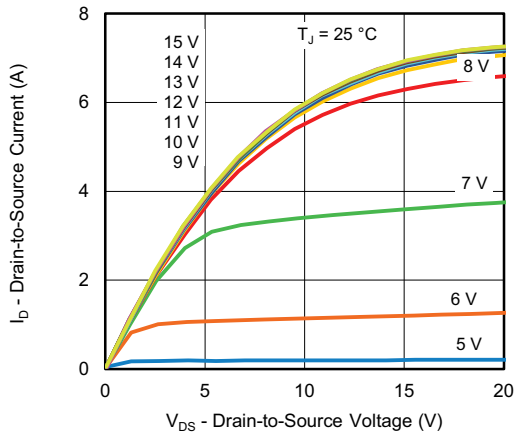


Fig. 1 - Typical Output Characteristics

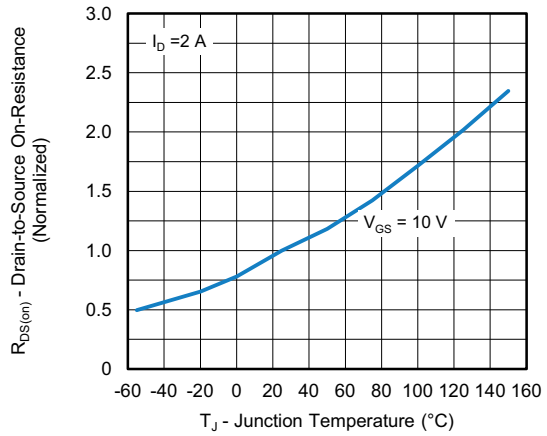


Fig. 4 - Normalized On-Resistance vs. Temperature

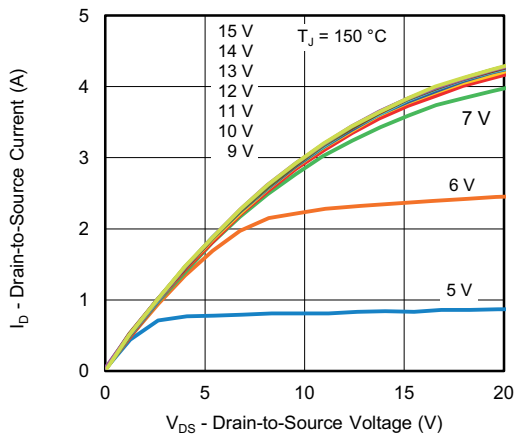


Fig. 2 - Typical Output Characteristics

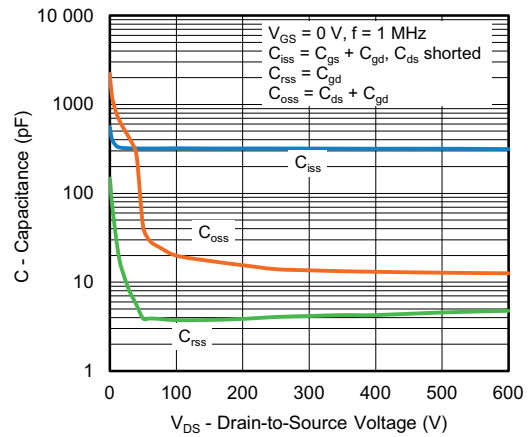


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

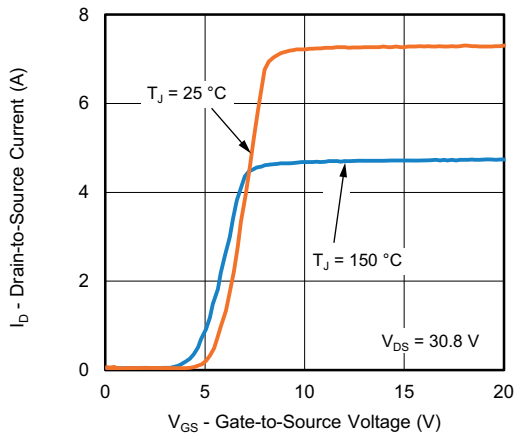


Fig. 3 - Typical Transfer Characteristics

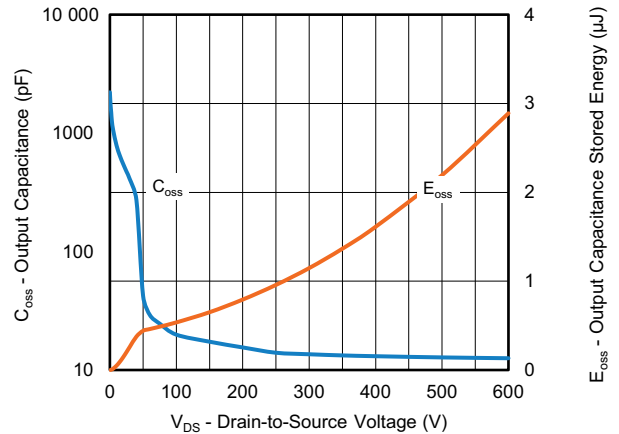


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

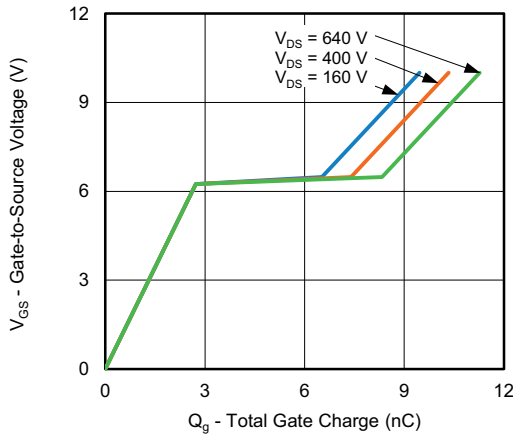


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

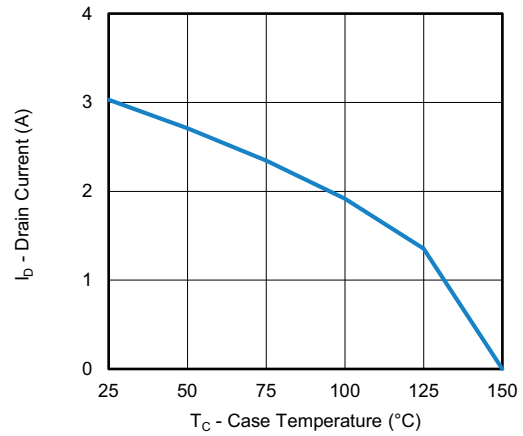


Fig. 10 - Maximum Drain Current vs. Case Temperature

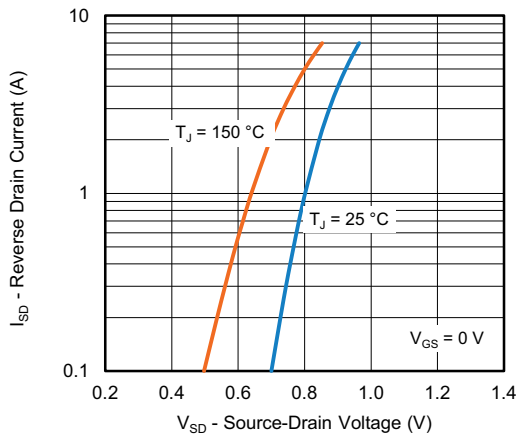


Fig. 8 - Typical Source-Drain Diode Forward Voltage

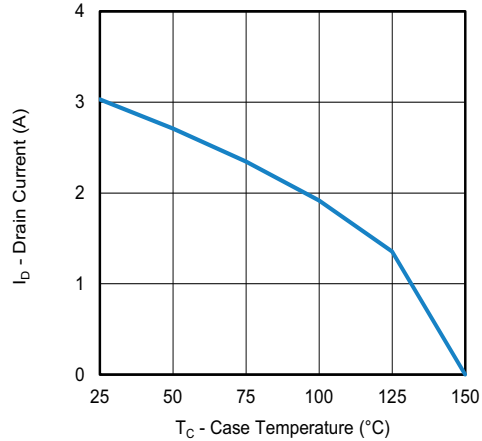


Fig. 11 - Normalized Breakdown Voltage vs. Temperature

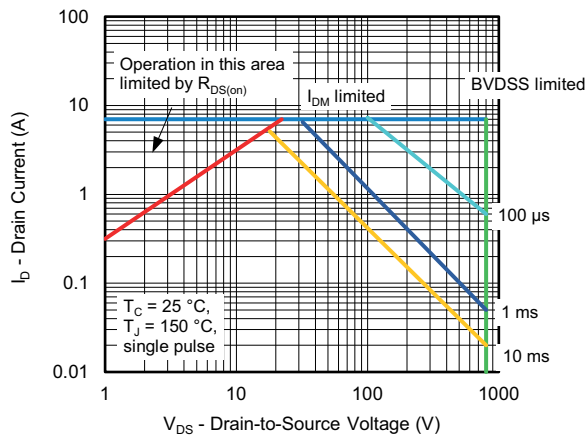


Fig. 9 - Maximum Safe Operating Area

Note

- a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

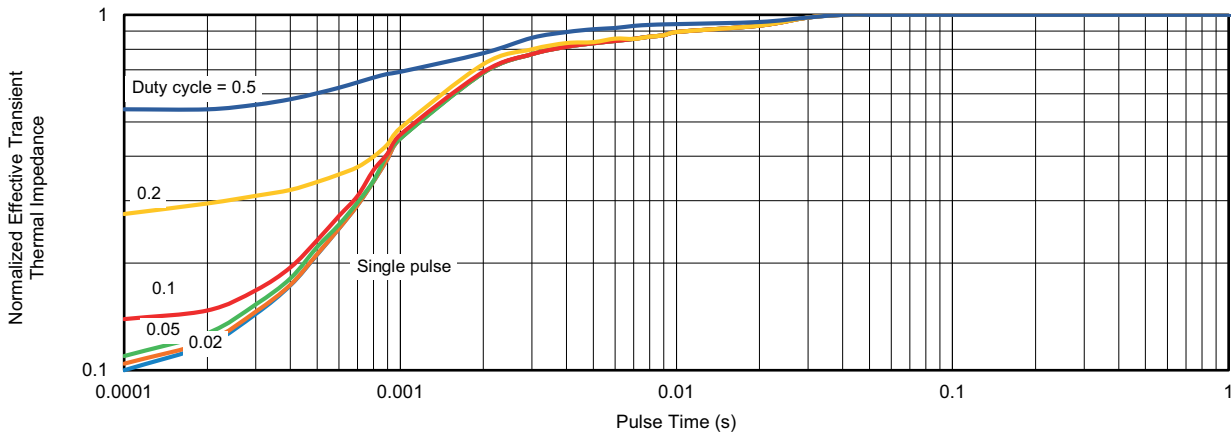


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

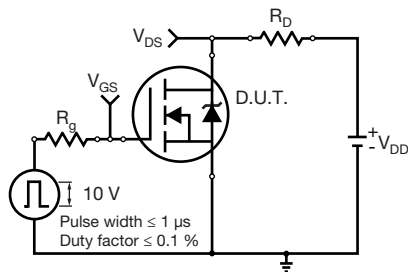


Fig. 13 - Switching Time Test Circuit

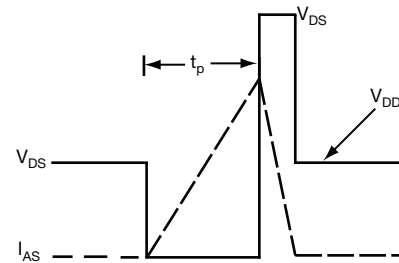


Fig. 16 - Unclamped Inductive Waveforms

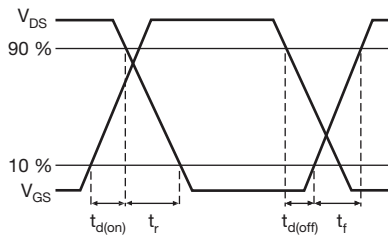


Fig. 14 - Switching Time Waveforms

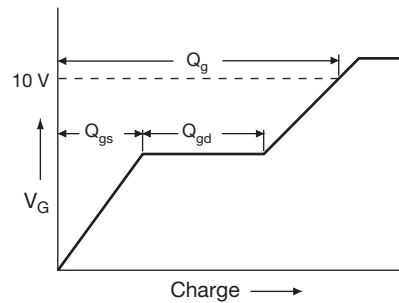


Fig. 17 - Basic Gate Charge Waveform

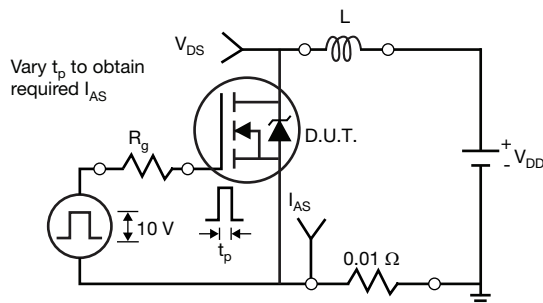


Fig. 15 - Unclamped Inductive Test Circuit

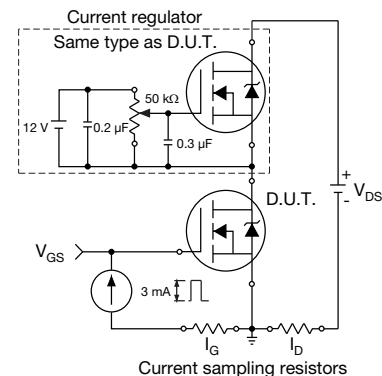


Fig. 18 - Gate Charge Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 19 - For N-Channel

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TO-220 FULLPAK Thin Lead



SYMBOL	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.30	4.70	0.169	0.185
A1	2.50	2.90	0.098	0.114
A2	2.40	2.80	0.094	0.110
b	0.60	0.80	0.024	0.031
b2	0.60	0.90	0.024	0.035
c	-	0.60	-	0.024
D	8.30	8.70	0.327	0.342
d1	14.70	15.30	0.579	0.602
d2	2.90	3.10	0.114	0.122
d3	3.30	3.70	0.130	0.146
E	9.70	10.30	0.382	0.406
e	2.50	2.70	0.098	0.106
L	13.40	13.80	0.528	0.543
L1	1.00	2.80	0.039	0.110
$\varnothing P$	3.00	3.40	0.118	0.134

ECN: E20-0684-Rev. D, 28-Dec-2020
DWG: 6021



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