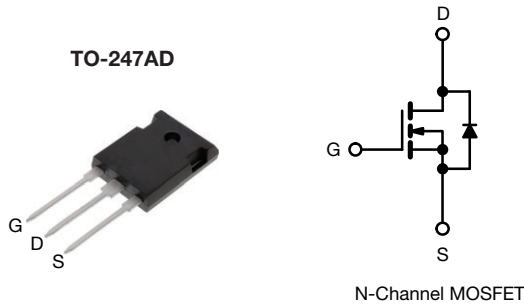


## E Series Power MOSFET With Fast Body Diode



### FEATURES

- Fast body diode MOSFET using E series technology
- Reduced  $t_{rr}$ ,  $Q_{rr}$ , and  $I_{RRM}$
- Low figure-of-merit (FOM):  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Low switching losses due to reduced  $Q_{rr}$
- 175 °C operating temperature
- AEC-Q101 qualified
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

 AUTOMOTIVE  
GRADE  
Available

**RoHS**  
COMPLIANT  
HALOGEN  
FREE

### APPLICATIONS

- Automotive onboard charger
- Automotive DC/DC converter

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	700	
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.063
$Q_g$ typ. (nC)	177	
$Q_{gs}$ (nC)	46	
$Q_{gd}$ (nC)	68	
Configuration	Single	

### ORDERING INFORMATION

Package	TO-247AD
Lead (Pb)-free and halogen-free	SQW44N65EF-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	650	V	
Gate-source voltage	$V_{GS}$	$\pm 30$		
Continuous drain current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	47	A
		$T_C = 100$ °C	34	
Pulsed drain current <sup>a</sup>	$I_{DM}$	146		
Linear derating factor		3.3	W/°C	
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	596	mJ	
Maximum power dissipation	$P_D$	500	W	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C	
Drain-source voltage slope	$dv/dt$	$T_J = 125$ °C	100	V/ns
Reverse diode $dv/dt$ <sup>d</sup>		50		
Soldering recommendations (peak temperature) <sup>c</sup>	for 10 s	260	°C	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 6.5$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $di/dt = 145$  A/ $\mu$ s, starting  $T_J = 25$  °C

### THERMAL RESISTANCE RATINGS

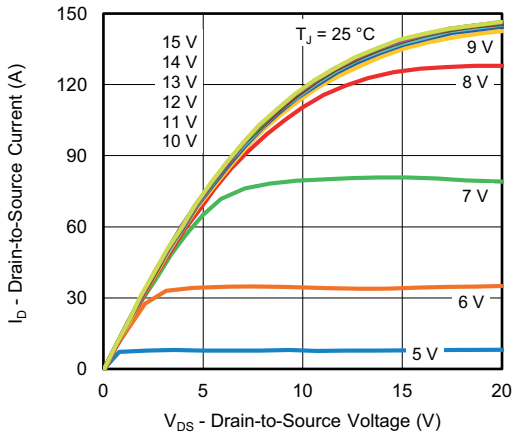
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	40	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	0.3	

<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	650	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 10\text{ mA}$	-	0.7	-	V/ $^\circ\text{C}$
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 520\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 520\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$	-	-	500	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 22\text{ A}$	-	0.063	0.073	$\Omega$
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 30\text{ V}$ , $I_D = 22\text{ A}$	-	18	-	S
<b>Dynamic</b>						
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$	-	5858	-	pF
Output capacitance	$C_{oss}$		-	227	-	
Reverse transfer capacitance	$C_{rss}$		-	6	-	
Effective output capacitance, energy related <sup>a</sup>	$C_{o(er)}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ V to } 520\text{ V}$	-	173	-	pF
Effective output capacitance, time related <sup>b</sup>	$C_{o(tr)}$		-	710	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}$ , $I_D = 22\text{ A}$ , $V_{DS} = 520\text{ V}$	-	177	266	nC
Gate-source charge	$Q_{gs}$		-	46	-	
Gate-drain charge	$Q_{gd}$		-	68	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 520\text{ V}$ , $I_D = 22\text{ A}$ , $R_g = 9.1\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	47	94	ns
Rise time	$t_r$		-	71	142	
Turn-off delay time	$t_{d(off)}$		-	206	412	
Fall time	$t_f$		-	66	132	
Gate input resistance	$R_g$	$f = 1\text{ MHz}$ , open drain	0.5	1.0	2.0	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	47	A
Pulsed diode forward current	$I_{SM}$		-	-	146	
Diode forward voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 22\text{ A}$ , $V_{GS} = 0\text{ V}$	-	0.9	1.2	V
Reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = I_S = 22\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_R = 400\text{ V}$	-	190	380	ns
Reverse recovery charge	$Q_{rr}$		-	1.7	3.4	$\mu\text{C}$
Reverse recovery current	$I_{RRM}$		-	17	-	A

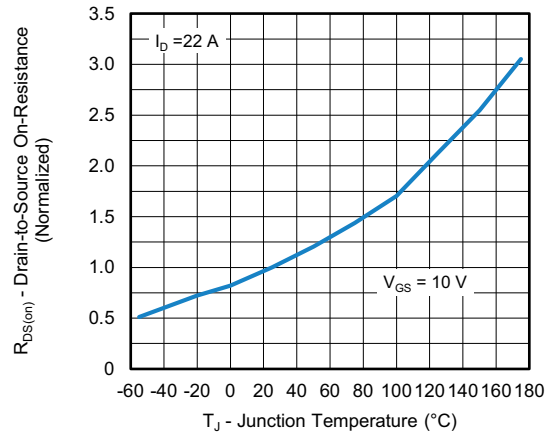
**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$   
 b.  $C_{oss(tr)}$  is a fixed capacitance that gives the charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$

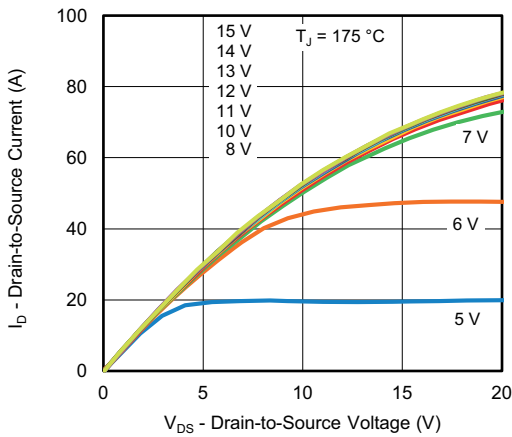
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



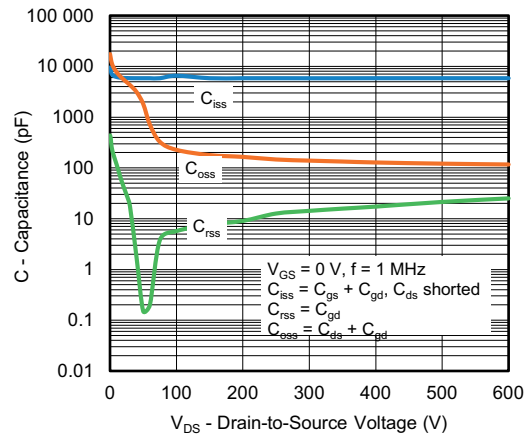
**Fig. 1 - Typical Output Characteristics**



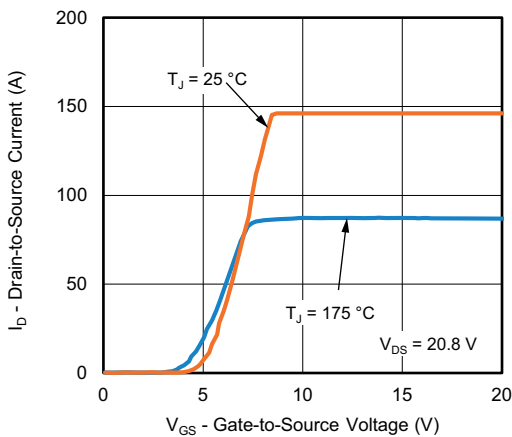
**Fig. 4 - Normalized On-Resistance vs. Temperature**



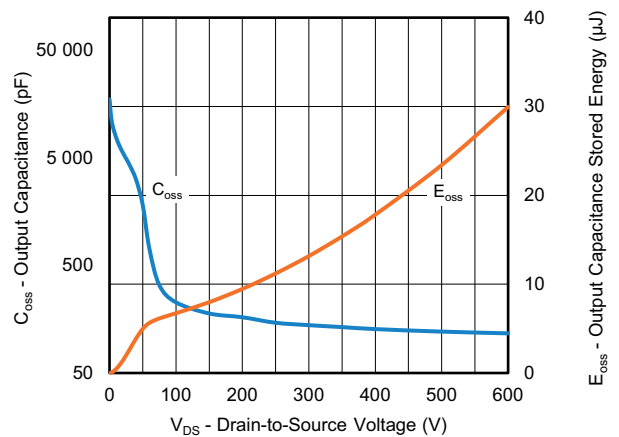
**Fig. 2 - Typical Output Characteristics**



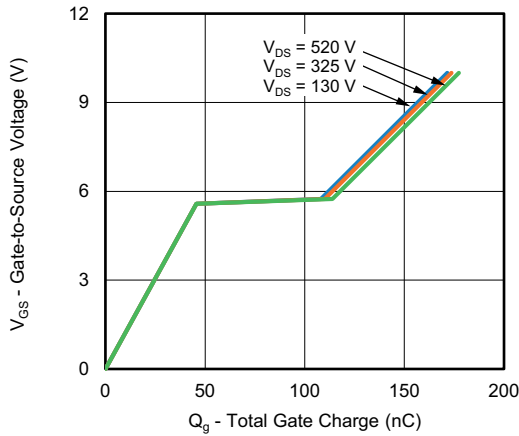
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



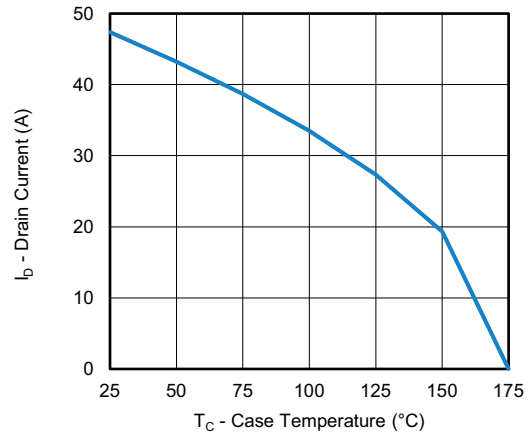
**Fig. 3 - Typical Transfer Characteristics**



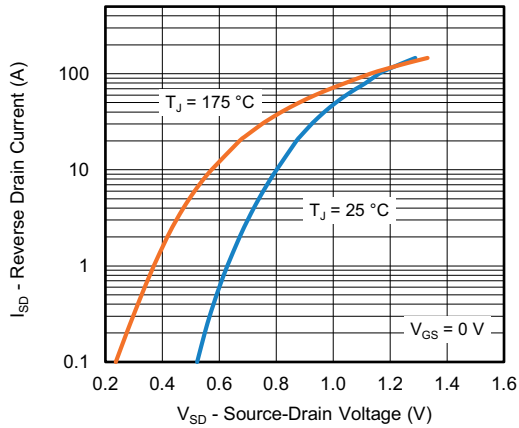
**Fig. 6 - C<sub>oss</sub> and E<sub>oss</sub> vs. V<sub>DS</sub>**



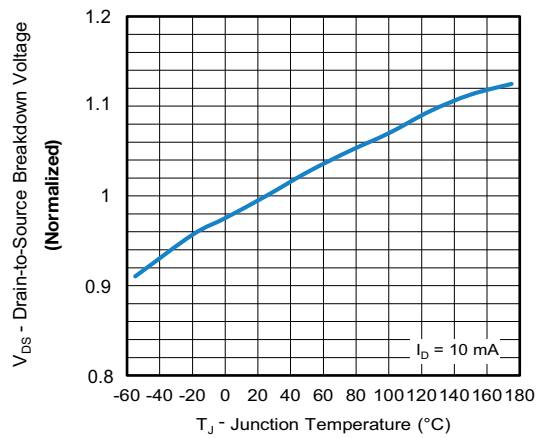
**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**



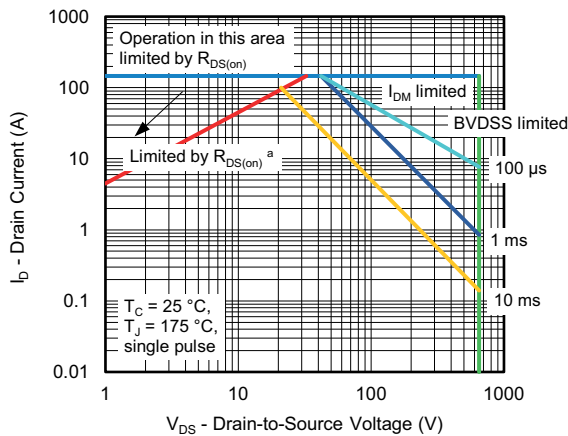
**Fig. 10 - Maximum Drain Current vs. Case Temperature**



**Fig. 8 - Typical Source-Drain Diode Forward Voltage**



**Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature**



**Fig. 9 - Maximum Safe Operating Area**

**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

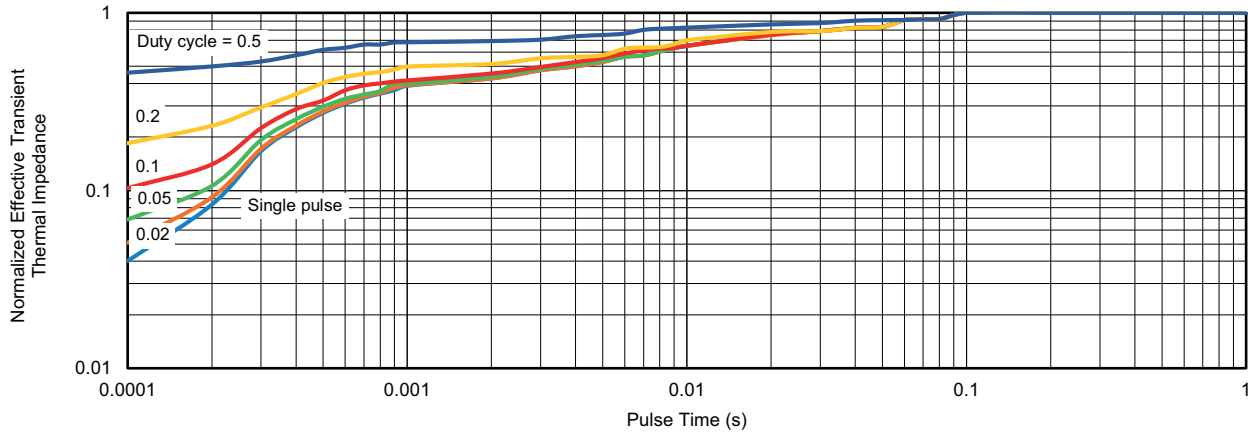


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

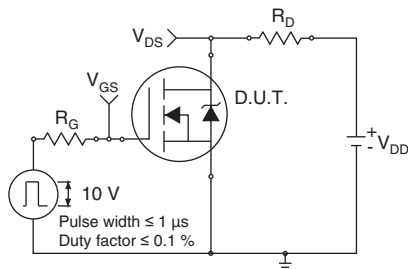


Fig. 13 - Switching Time Test Circuit

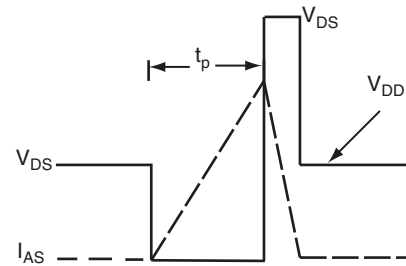


Fig. 16 - Unclamped Inductive Waveforms

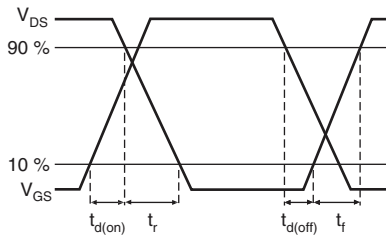


Fig. 14 - Switching Time Waveforms

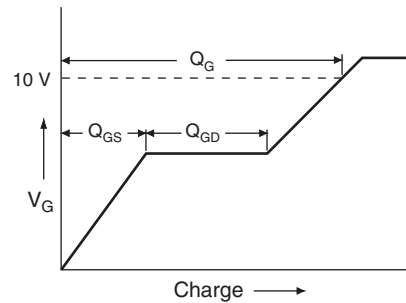


Fig. 17 - Basic Gate Charge Waveform

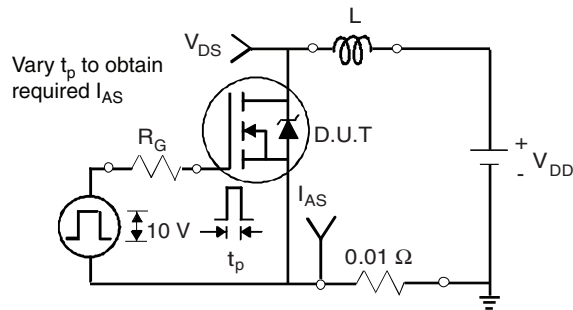


Fig. 15 - Unclamped Inductive Test Circuit

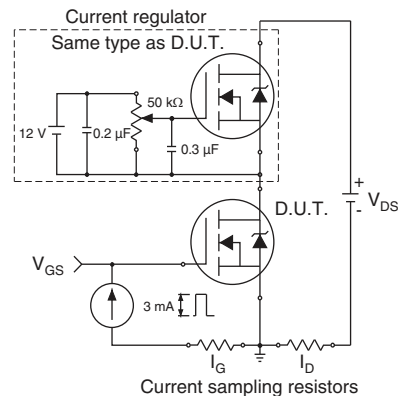
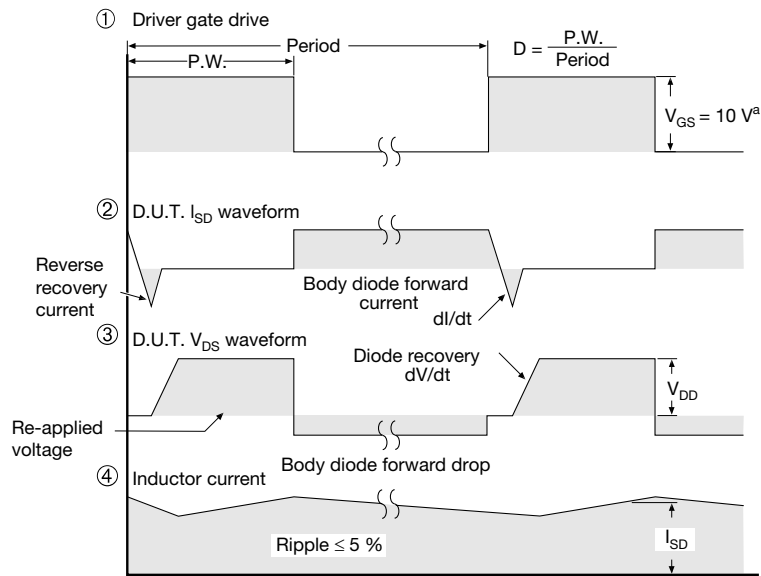
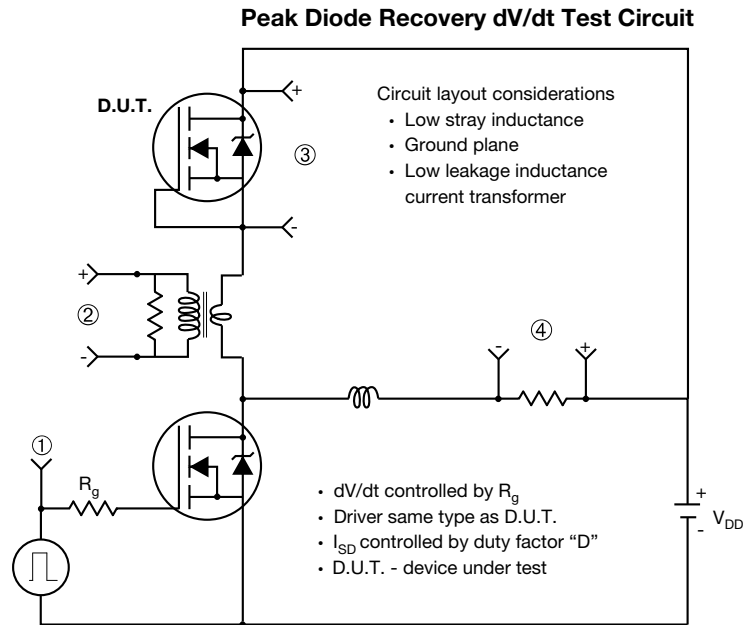


Fig. 18 - Gate Charge Test Circuit

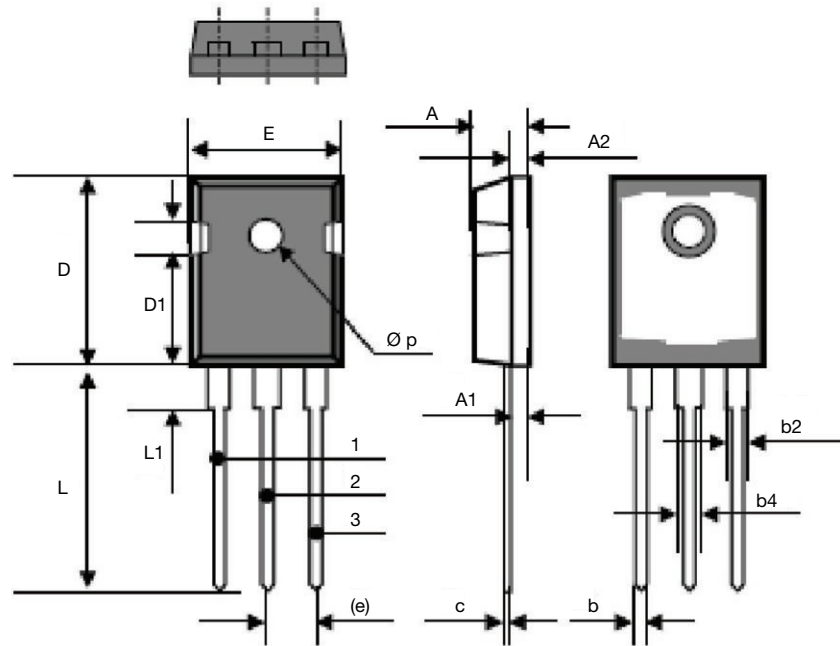


**Note**  
a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 19 - For N-Channel**

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## TO-247AD (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.31	0.185	0.209
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	0.99	1.40	0.039	0.055
b2	1.65	2.41	0.065	0.095
b4	2.59	3.43	0.102	0.135
c	0.61 BSC		0.024 BSC	
D	20.80	21.46	0.819	0.845
D1	3.68	5.49	0.145	0.216
(e)	5.46 BSC		0.215 BSC	
E	15.49	16.26	0.610	0.640
L	19.81	20.32	0.780	0.800
L1	4.06	4.50	0.160	0.177
Ø p	3.51	3.66	0.138	0.144

ECN: S17-0178-Rev. B, 06-Feb-17  
 DWG: 6010



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