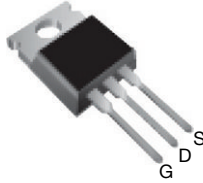


## Power MOSFET

**TO-220AB**


N-Channel MOSFET

### FEATURES

- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low effective capacitance ( $C_{o(er)}$ )
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Solar (PV inverters)

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	550	
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.740
$Q_g$ max. (nC)	39	
$Q_{gs}$ (nC)	9	
$Q_{gd}$ (nC)	12	
Configuration	Single	

### ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free and halogen-free	IRF840HPBF

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	500	V	
Gate-source voltage	$V_{GS}$	$\pm 30$		
Continuous drain current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	7.3	A
		$T_C = 100$ °C	4.6	
Pulsed drain current <sup>a</sup>	$I_{DM}$	17		
Linear derating factor		1.0	W/°C	
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	175	mJ	
Maximum power dissipation	$P_D$	125	W	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C	
Drain-source voltage slope	dv/dt	$T_J = 125$ °C	100	V/ns
Reverse diode dv/dt <sup>d</sup>		0.2		
Soldering recommendations (peak temperature) <sup>c</sup>	For 10 s	260	°C	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 120$  V, starting  $T_J = 25$  °C,  $L = 14$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 5$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $di/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R <sub>thJA</sub>	-	62	°C/W
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	1.0	

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		500	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.56	-	V/°C
Gate-source threshold voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	100	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.8 A	-	0.740	0.850	Ω
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 4.8 A		-	2.8	-	S
<b>Dynamic</b>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		-	1059	-	pF
Output capacitance	C <sub>oss</sub>			-	125	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	14	-	
Effective output capacitance, energy related <sup>a</sup>	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V		-	40	-	pF
Effective output capacitance, time related <sup>b</sup>	C <sub>o(tr)</sub>			-	72	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 8 A, V <sub>DS</sub> = 400 V	-	26	39	nC
Gate-source charge	Q <sub>gs</sub>			-	9	-	
Gate-drain charge	Q <sub>gd</sub>			-	12	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 8 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	15	30	ns
Rise time	t <sub>r</sub>			-	30	60	
Turn-off delay time	t <sub>d(off)</sub>			-	23	46	
Fall time	t <sub>f</sub>			-	17	34	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain		0.5	1.0	2.0	Ω
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	7.3	A
Pulsed diode forward current	I <sub>SM</sub>			-	-	17	
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 8 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 8 A, di/dt = 100 A/μs, V <sub>R</sub> = 25 V		-	441	882	ns
Reverse recovery charge	Q <sub>rr</sub>			-	2.9	5.8	μC
Reverse recovery current	I <sub>RRM</sub>			-	12	-	A

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

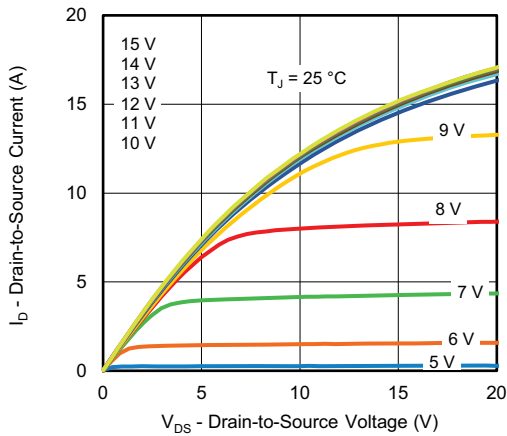


Fig. 1 - Typical Output Characteristics

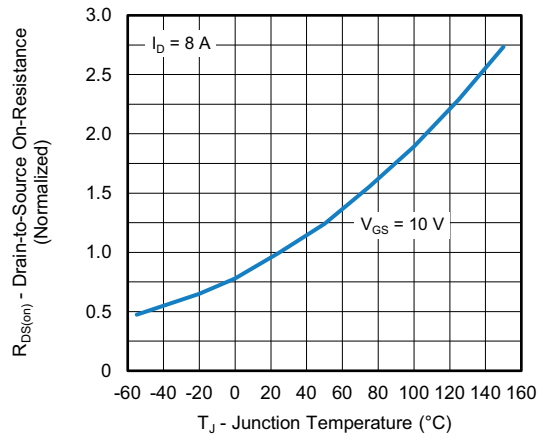


Fig. 4 - Normalized On-Resistance vs. Temperature

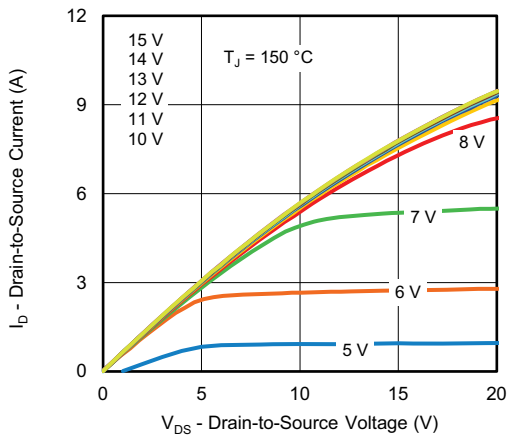


Fig. 2 - Typical Output Characteristics

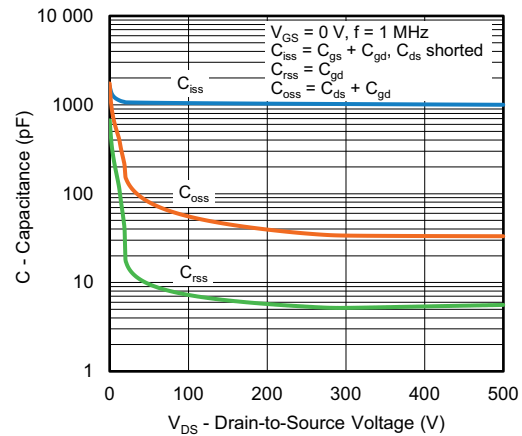


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

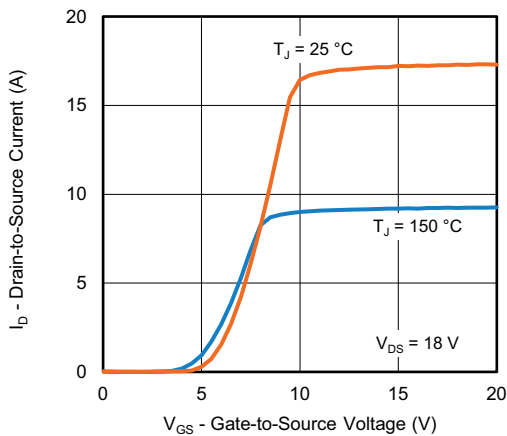


Fig. 3 - Typical Transfer Characteristics

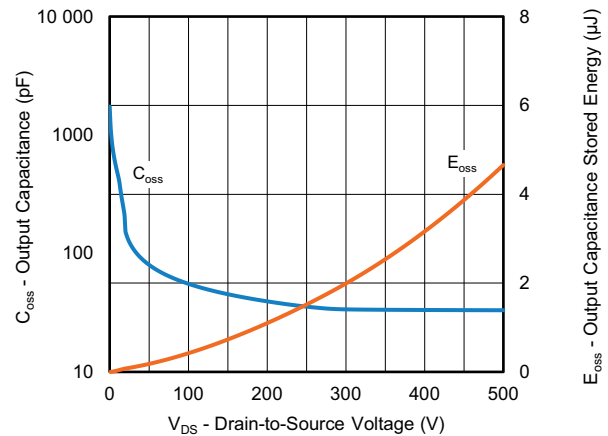


Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$

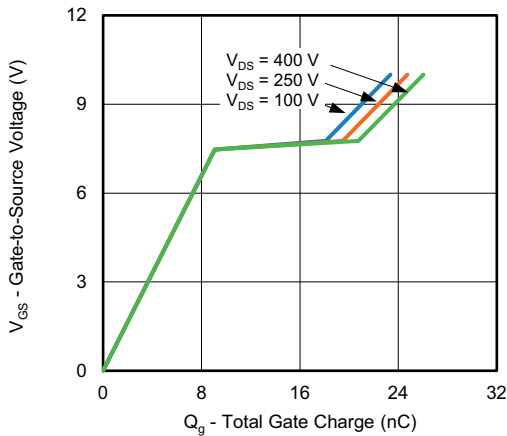


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

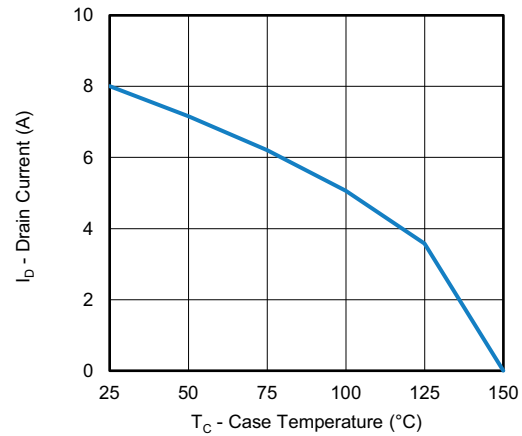


Fig. 10 - Maximum Drain Current vs. Case Temperature

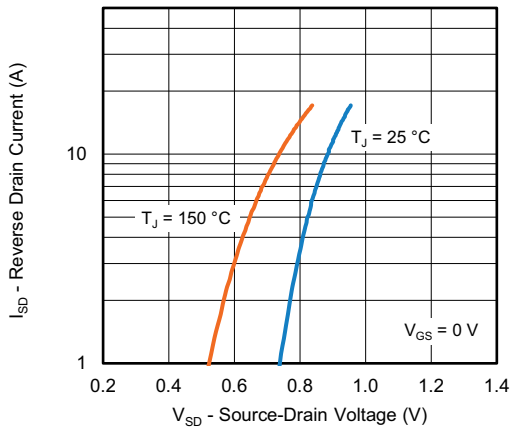


Fig. 8 - Typical Source-Drain Diode Forward Voltage

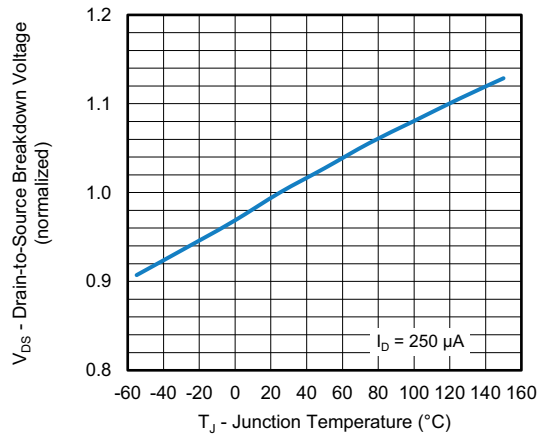


Fig. 11 - Temperature vs. Drain-to-Source Voltage

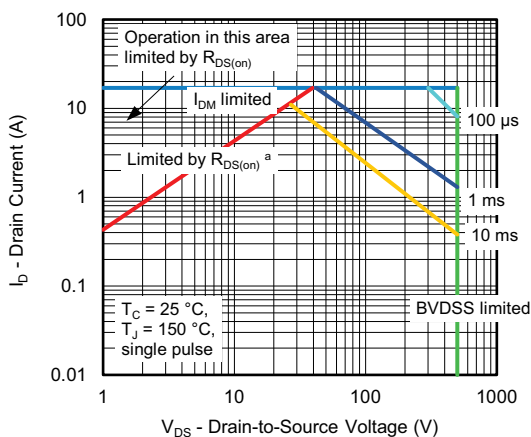


Fig. 9 - Maximum Safe Operating Area

**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

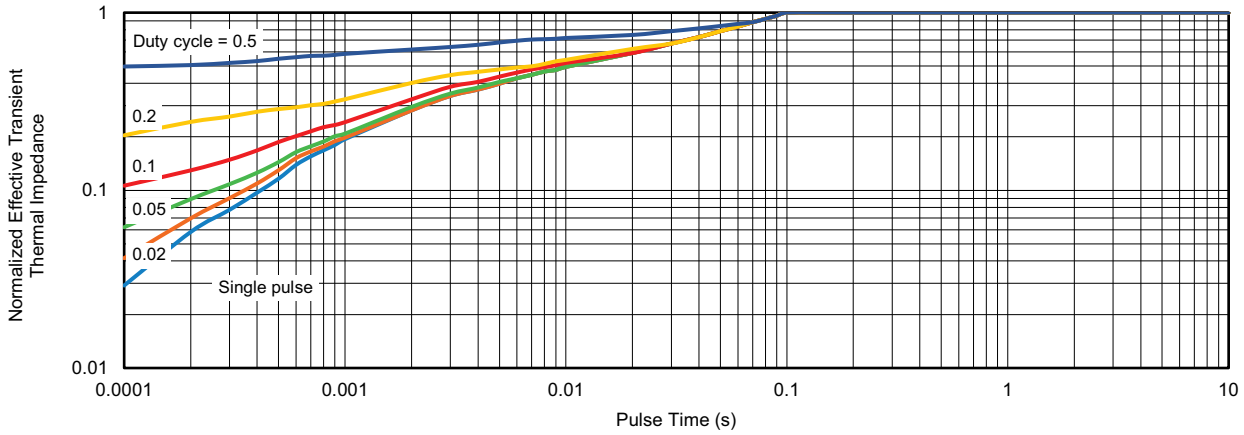


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

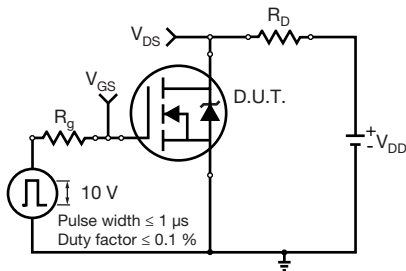


Fig. 13 - Switching Time Test Circuit

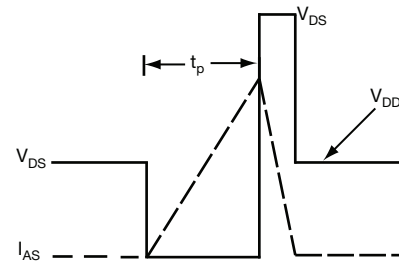


Fig. 16 - Unclamped Inductive Waveforms

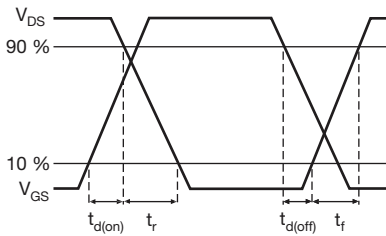


Fig. 14 - Switching Time Waveforms

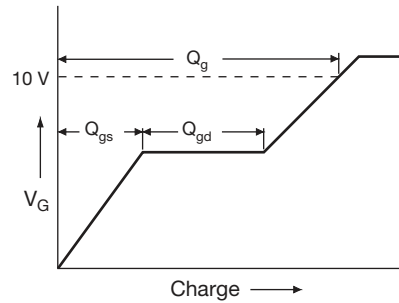


Fig. 17 - Basic Gate Charge Waveform

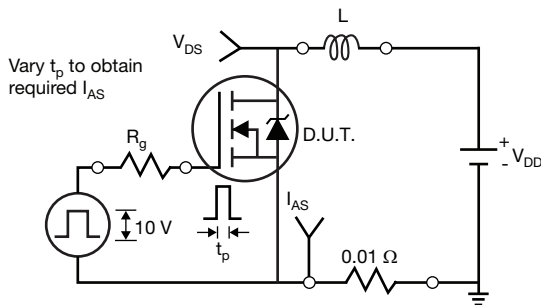


Fig. 15 - Unclamped Inductive Test Circuit

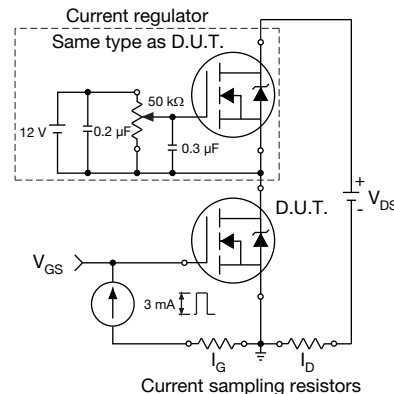


Fig. 18 - Gate Charge Test Circuit



**Note**  
 a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 19 - For N-Channel**

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