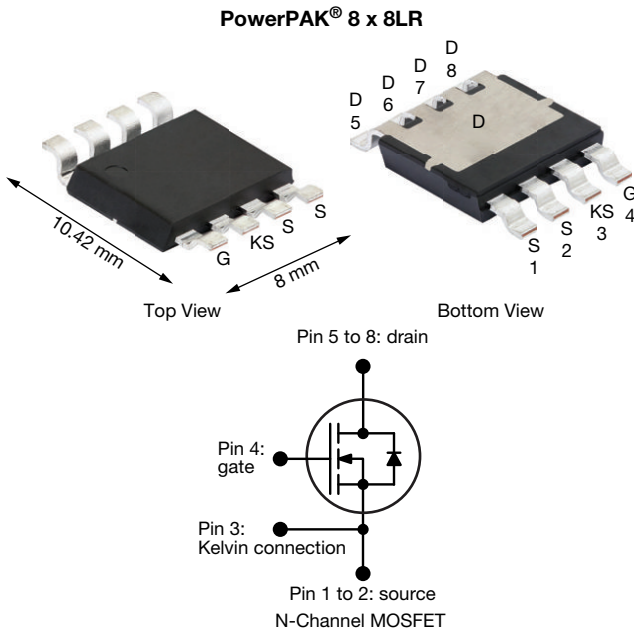


E Series Power MOSFET



FEATURES

- 4th generation E series technology
- Low figure of merit (FOM) $R_{on} \times Q_g$
- Low effective capacitance ($C_{o(er)}$)
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

PRODUCT SUMMARY	
V_{DS} (V) at T_J max.	650
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V 0.074
Q_g max. (nC)	63
Q_{gs} (nC)	19
Q_{gd} (nC)	10
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 8 x 8LR
Lead (Pb)-free and halogen-free	SiHR080N60E-T1-GE3


ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	600	V	
Gate-source voltage	V_{GS}	± 30		
Continuous drain current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	51	A
		$T_C = 100$ °C	32	
Pulsed drain current ^a	I_{DM}	96		
Linear derating factor		4.0	W/°C	
Single pulse avalanche energy ^b	E_{AS}	173	mJ	
Maximum power dissipation	P_D	500	W	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C	
Drain-source voltage slope	dv/dt	$T_J = 125$ °C	100	V/ns
Reverse diode dv/dt ^d			10	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{PD} = 120$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 3.5$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $di/dt = 100$ A/ μ s, starting $T_J = 25$ °C



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	42	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.25	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$		-	0.64	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$		-	-	± 1	μA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 17\text{ A}$	-	0.074	0.084	Ω
Forward transconductance ^a	g_{fs}	$V_{DS} = 20\text{ V}, I_D = 17\text{ A}$		-	4.6	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$		-	2557	-	pF
Output capacitance	C_{oss}			-	105	-	
Reverse transfer capacitance	C_{rss}			-	6	-	
Effective output capacitance, energy related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$		-	79	-	pF
Effective output capacitance, time related ^b	$C_{o(tr)}$			-	499	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 17\text{ A}, V_{DS} = 480\text{ V}$	-	42	63	nC
Gate-source charge	Q_{gs}			-	19	-	
Gate-drain charge	Q_{gd}			-	10	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 480\text{ V}, I_D = 17\text{ A}, V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$		-	31	62	ns
Rise time	t_r			-	96	144	
Turn-off delay time	$t_{d(off)}$			-	37	74	
Fall time	t_f			-	31	62	
Gate input resistance	R_g	$f = 1\text{ MHz}$		0.3	0.7	1.4	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	51	A
Pulsed diode forward current	I_{SM}			-	-	96	
Diode forward voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 17\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.2	V
Reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 17\text{ A}, di/dt = 80\text{ A}/\mu\text{s}, V_R = 25\text{ V}$		-	441	882	ns
Reverse recovery charge	Q_{rr}			-	5.2	10.4	μC
Reverse recovery current	I_{RRM}			-	21	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
- b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

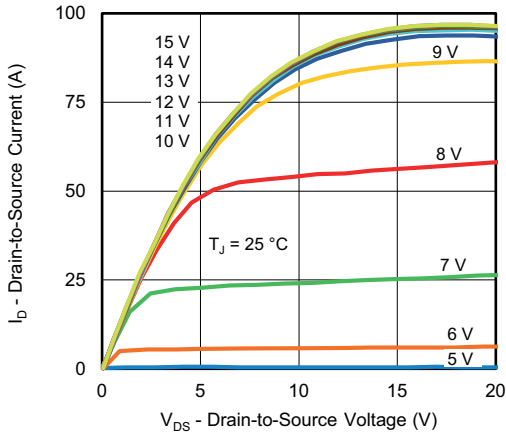


Fig. 1 - Typical Output Characteristics

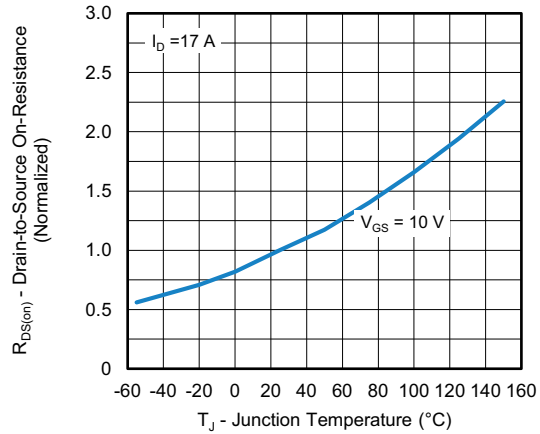


Fig. 4 - Normalized On-Resistance vs. Temperature

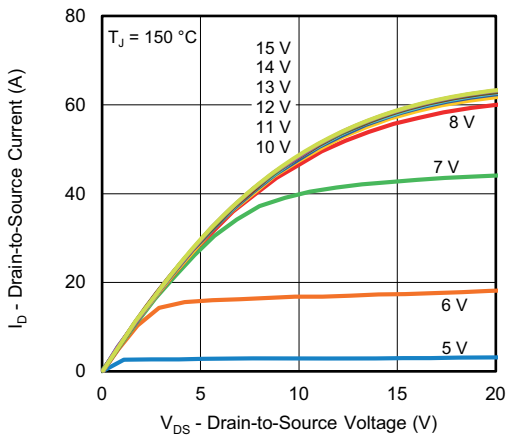


Fig. 2 - Typical Output Characteristics

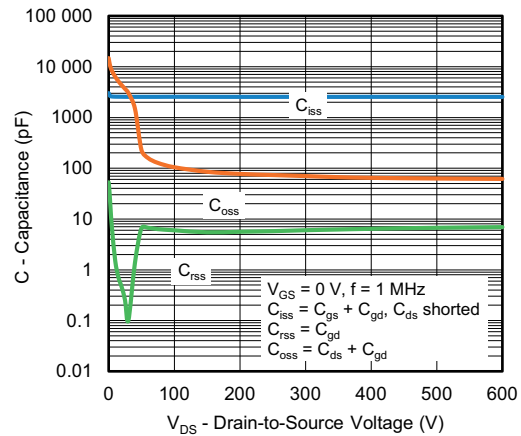


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

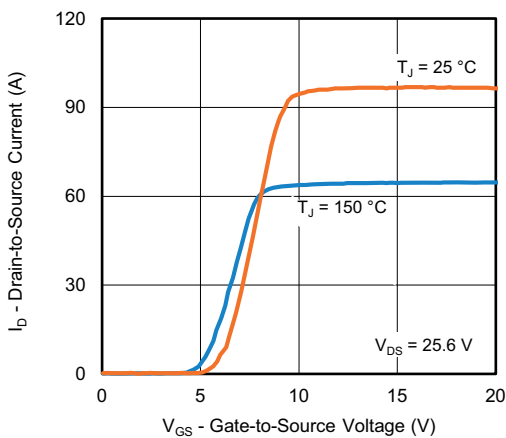


Fig. 3 - Typical Transfer Characteristics

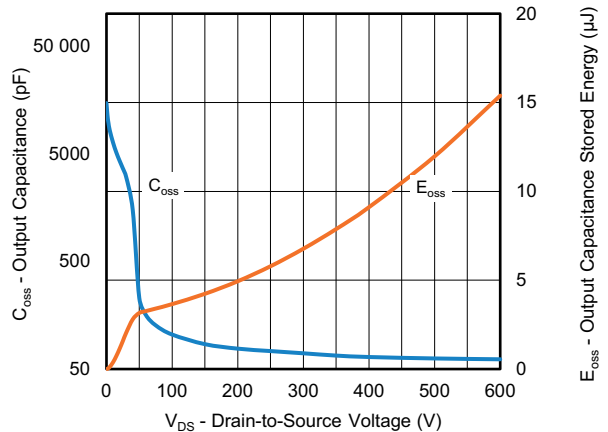


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

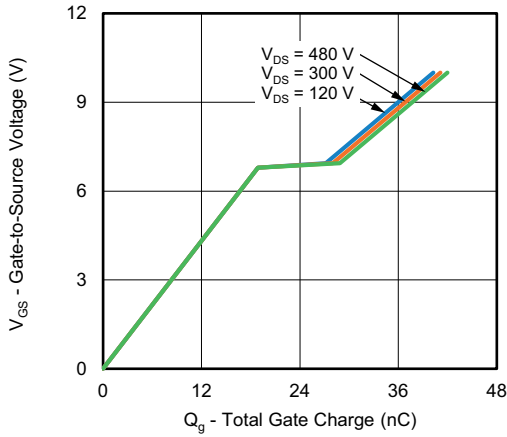


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

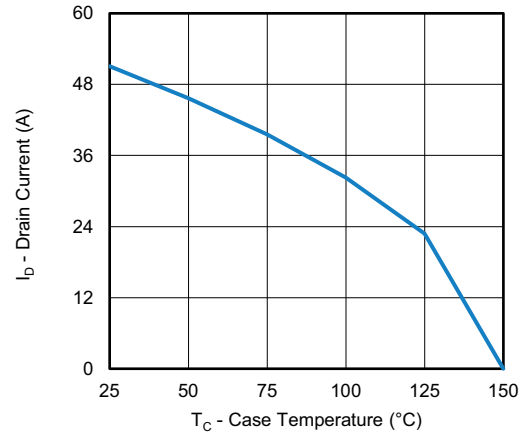


Fig. 10 - Maximum Drain Current vs. Case Temperature

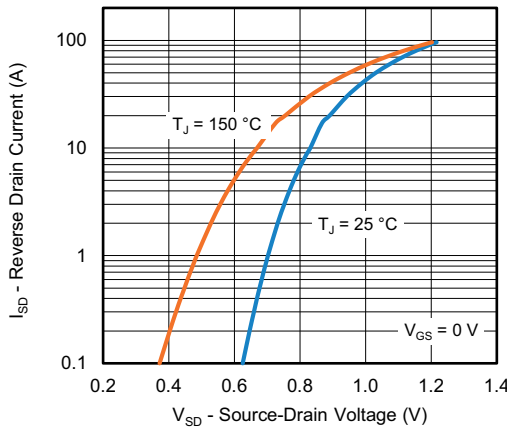


Fig. 8 - Typical Source-Drain Diode Forward Voltage

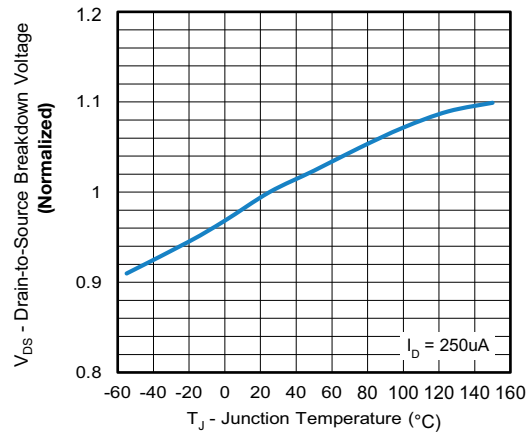


Fig. 11 - Temperature vs. Drain-to-Source Voltage

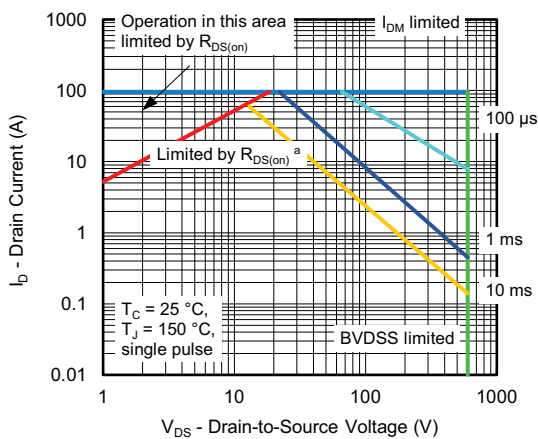


Fig. 9 - Maximum Safe Operating Area

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

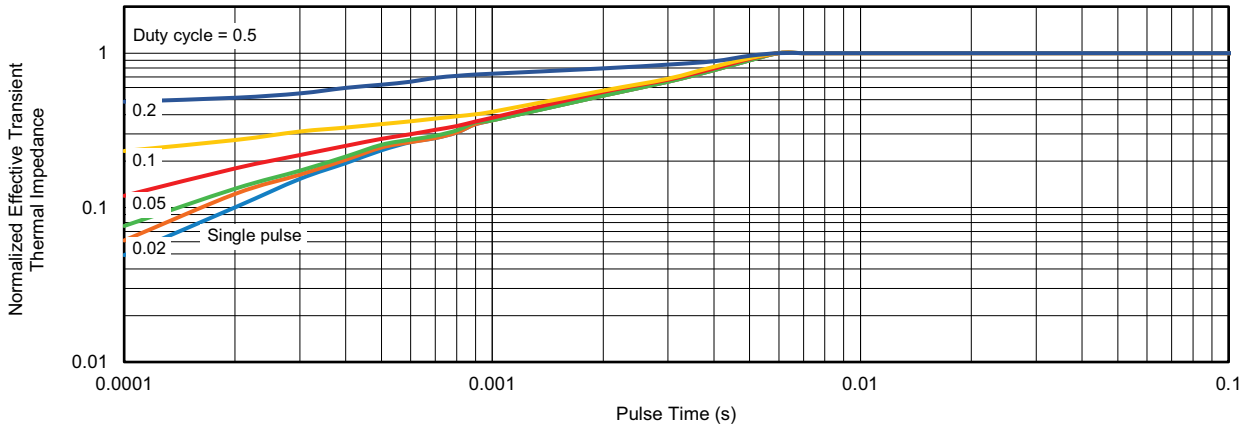


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

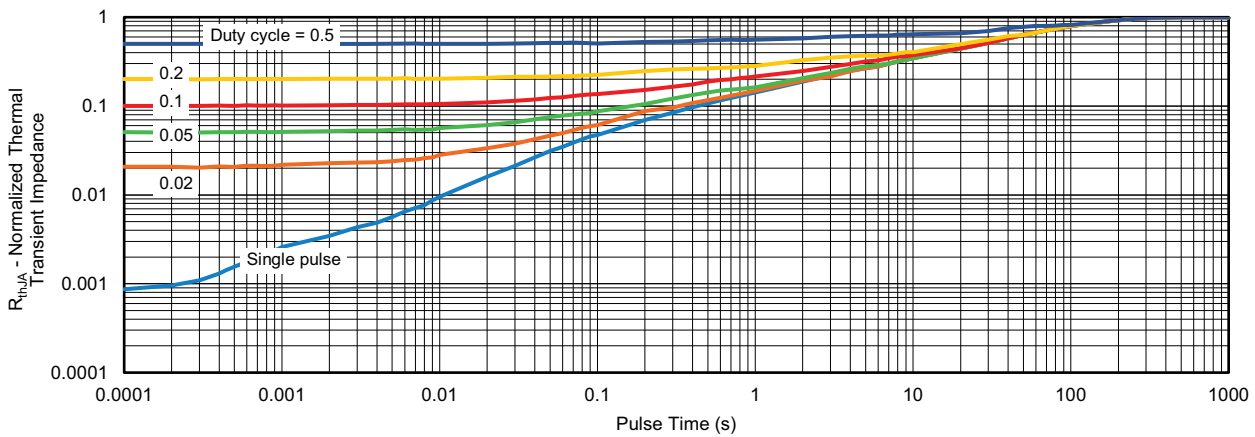


Fig. 13 - Normalized Transient Thermal Impedance, Junction-to-Ambient

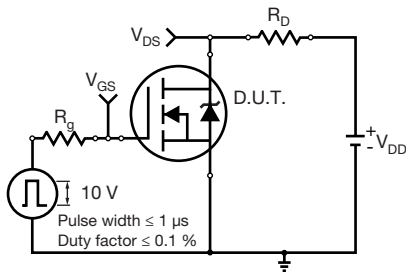


Fig. 14 - Switching Time Test Circuit

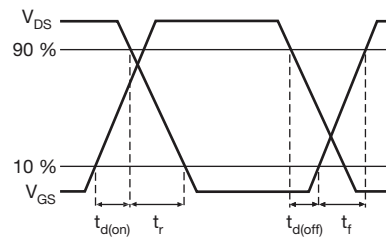


Fig. 15 - Switching Time Waveforms

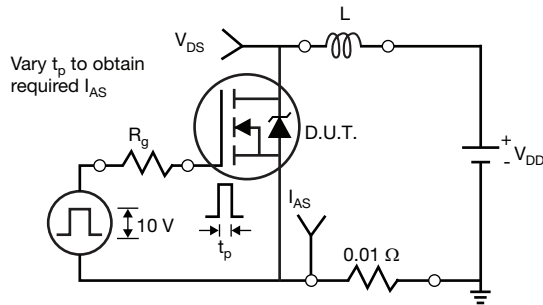


Fig. 16 - Unclamped Inductive Test Circuit

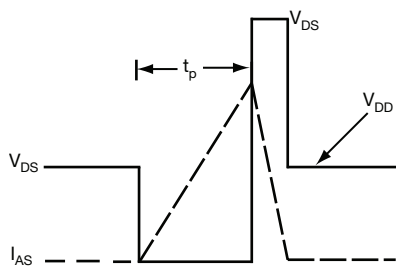


Fig. 17 - Unclamped Inductive Waveforms

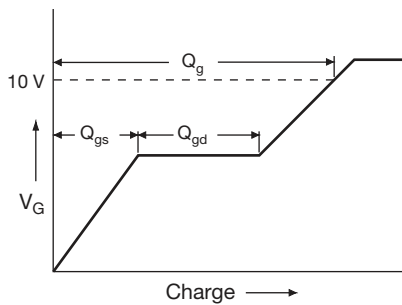


Fig. 18 - Basic Gate Charge Waveform

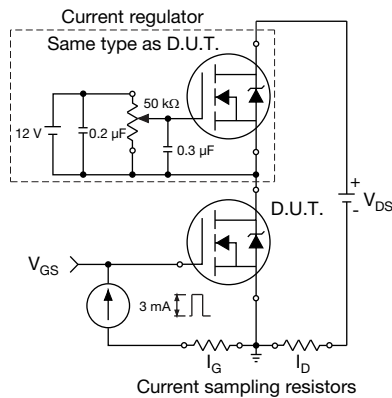
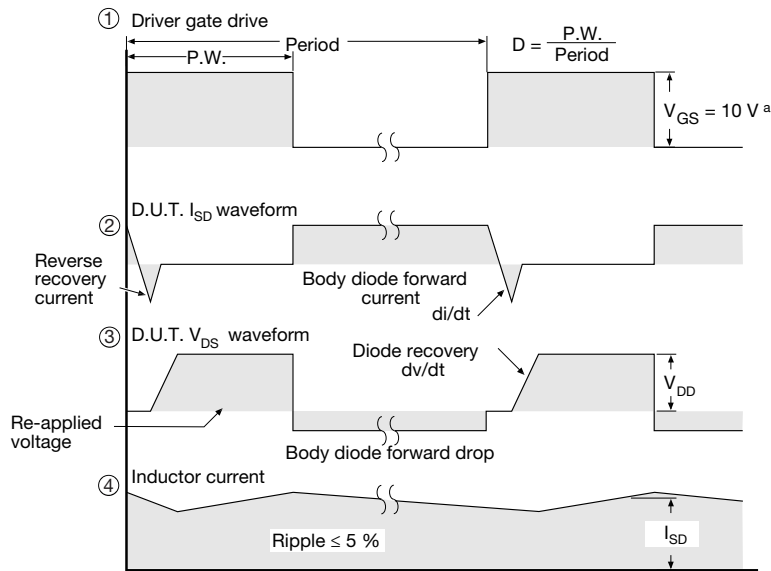
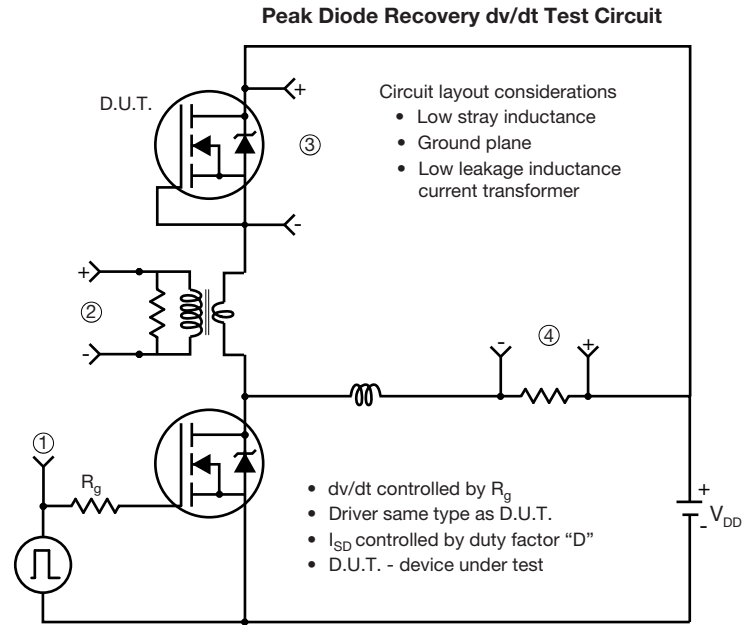


Fig. 19 - Gate Charge Test Circuit

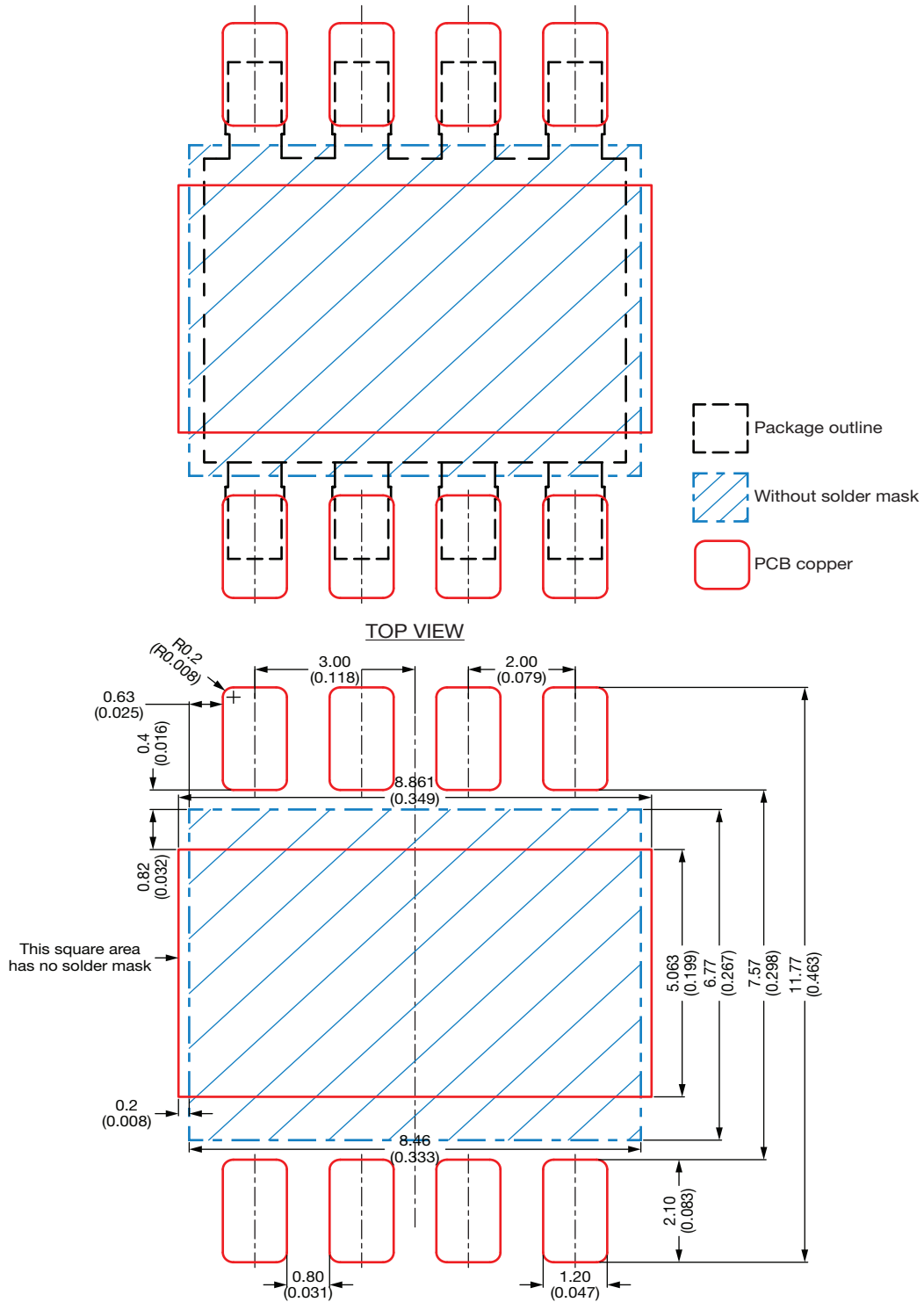


Note
 a. $V_{GS} = 5 V$ for logic level devices

Fig. 20 - For N-Channel

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Recommended Land Pattern PowerPAK® 8 x 8LR



Notes

- This land pattern is for reference
- Proposed stencil thickness 200 µm
- All dimensions are in millimeter (inches)

ECN: S23-1106-Rev. A, 11-Dec-2023
 DWG: 3022



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