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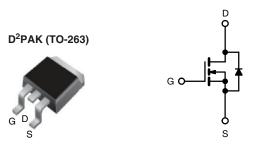
Vishay Siliconix

COMPLIANT

HALOGEN

FREE

EF Series Power MOSFET With Fast Body Diode



N_Channal	MOSEET

PRODUCT SUMMARY				
V _{DS} (V) at T _J max. 650				
R _{DS(on)} typ. (Ω) at 25 °C	$V_{GS} = 10 \text{ V}$	0.137		
Q _g max. (nC)	3	38		
Q _{gs} (nC)	1	10		
Q _{gd} (nC)	6			
Configuration	Single			

FEATURES

- 4th generation E series technology
- Low figure-of-merit (FOM) Ron x Qg
- Low effective capacitance (Co(er))
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

ORDERING INFORMATION	
Package	D ² PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHB155N60EF-GE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V_{DS}	600	V	
Gate-source voltage			V_{GS}	± 30		
Continuous drain surrent (T. – 150 °C)	V _{GS} at 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$	- I _D	21	А	
Continuous drain current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 100 °C		14		
Pulsed drain current ^a	I _{DM}	43				
Linear derating factor				1.42	W/°C	
Single pulse avalanche energy b			E _{AS}	111	mJ	
Maximum power dissipation			P _D	179	W	
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C	
Drain-source voltage slope $T_J = 125 ^{\circ}\text{C}$			dv/dt	100	V/ns	
Reverse diode dv/dt ^d				50] v/ns	
Soldering recommendations (peak temperature) ^c For 10 s				260	°C	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature
- b. V_{DD} = 120 V, starting T_J = 25 °C, L = 28.2 mH, R_q = 25 Ω , I_{AS} = 2.8 A
- c. 1.6 mm from case
- d. $I_{SD} \le I_D$, di/dt = 100 A/ μ s, starting $T_J = 25$ °C



Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R _{thJA}	-	62	°C/W	
Maximum junction-to-case (drain)	R_{thJC}	-	0.7	C/VV	

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static					•		
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		600	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = 1 mA	-	0.62	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = 250 μA	3.0	-	5.0	V
Cata aguirra laglaga		V _{GS} = ± 20 V		-	-	± 100	nA
Gate-source leakage	I_{GSS}	,	$V_{GS} = \pm 30 \text{ V}$	-	-	± 1	μA
Zava gata valtaga dvain avvvant		V _{DS} =	480 V, V _{GS} = 0 V	-	-	1	μΑ
Zero gate voltage drain current	I _{DSS}	V _{DS} = 480 V	, V _{GS} = 0 V, T _J = 125 °C	-	-	2	mA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A	-	0.137	0.159	Ω
Forward transconductance	9 _{fs}	V _{DS}	= 10 V, I _D = 10 A	-	9.2	-	S
Dynamic							
Input capacitance	C _{iss}		V _{GS} = 0 V,	-	1465	-	
Output capacitance	C _{oss}		$V_{DS} = 100 \text{ V},$	-	56	-	1
Reverse transfer capacitance	C _{rss}	f = 100 KHz		-	1	-	pF
Effective output capacitance, energy related	C _{o(er)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		-	61	-	
Effective output capacitance, time related	C _{o(tr)}			-	356	-	
Total gate charge	Qg		V _{GS} = 10 V		25	38	
Gate-source charge	Q _{gs}	V _{GS} = 10 V			10	-	nC
Gate-drain charge	Q _{gd}	1		-	6	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 480 V, I _D = 10 A,		-	20	40	
Rise time	t _r			-	27	54	
Turn-off delay time	t _{d(off)}	V _{GS} =	10 V, $R_g = 10.1 \Omega$	-	28	56	ns
Fall time	t _f		1		17	34	
Gate input resistance	R_g	f = 1 MHz, open drain		0.4	0.9	1.8	Ω
Drain-Source Body Diode Characteristic	s						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	21	
Pulsed diode forward current	I _{SM}			-	-	43	A .
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 10 A, V _{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t _{rr}			-	95	190	ns
Reverse recovery charge	Q _{rr}	$T_J = 25 \text{ °C}, I_F = I_S = 10 \text{ A},$ $di/dt = 100 \text{ A/µs}, V_R = 400 \text{ V}$		-	0.5	1.0	μC
Reverse recovery current	I _{RRM}			_	12	-	A



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

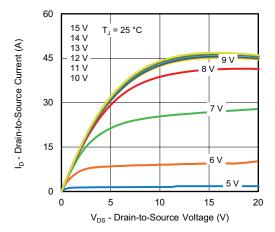


Fig. 1 - Typical Output Characteristics

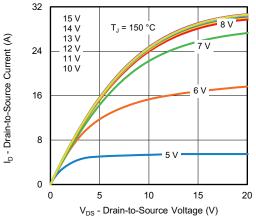


Fig. 2 - Typical Output Characteristics

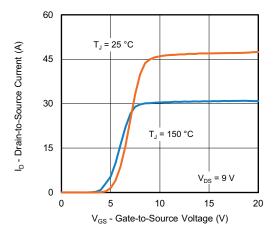


Fig. 3 - Typical Transfer Characteristics

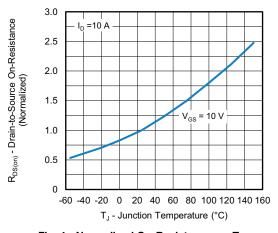


Fig. 4 - Normalized On-Resistance vs. Temperature

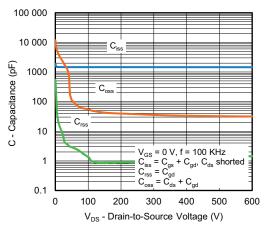


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

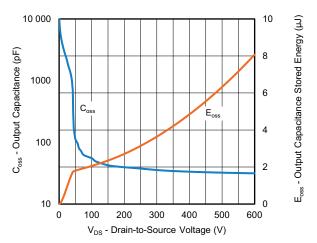


Fig. 6 - Coss and Eoss vs. VDS



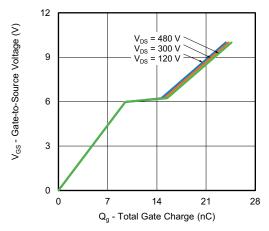


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

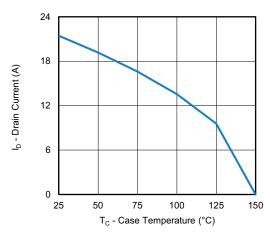


Fig. 9 - Maximum Drain Current vs. Case Temperature

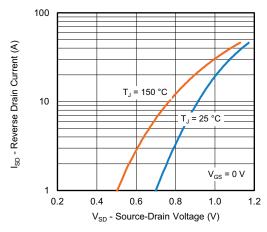


Fig. 8 - Typical Source-Drain Diode Forward Voltage

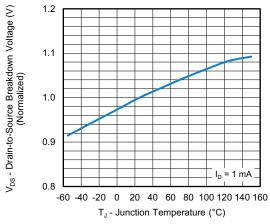


Fig. 10 - Temperature vs. Drain-to-Source Voltage

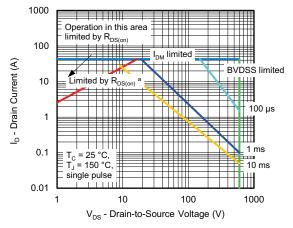


Fig. 11 - Maximum Safe Operating Area

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



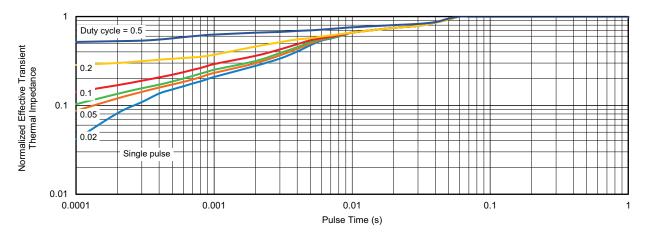


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

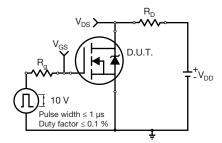


Fig. 13 - Switching Time Test Circuit

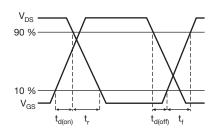


Fig. 14 - Switching Time Waveforms

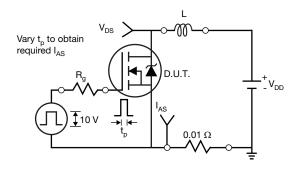


Fig. 15 - Unclamped Inductive Test Circuit

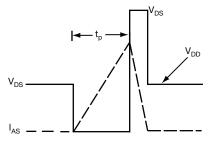


Fig. 16 - Unclamped Inductive Waveforms

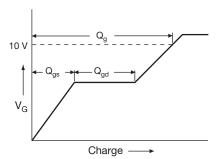


Fig. 17 - Basic Gate Charge Waveform

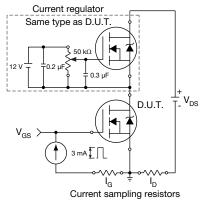
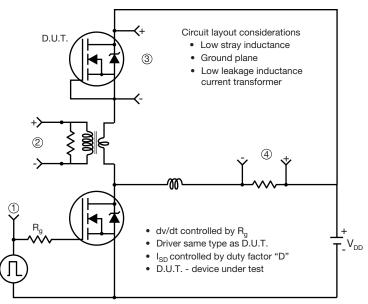


Fig. 18 - Gate Charge Test Circuit



Peak Diode Recovery dv/dt Test Circuit



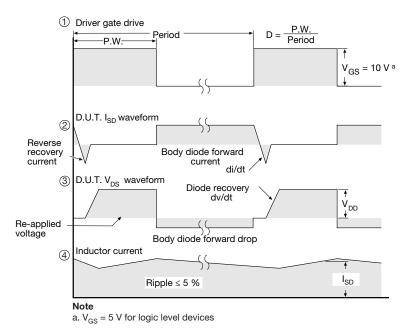


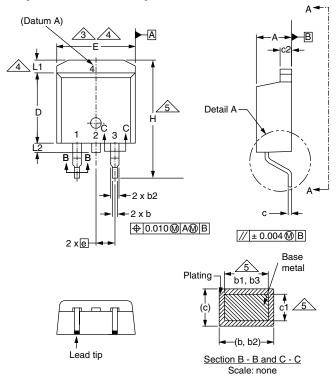
Fig. 19 - For N-Channel

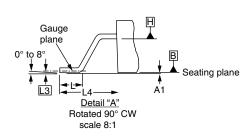
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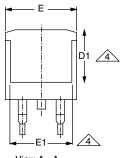




TO-263AB (HIGH VOLTAGE)







View A - A

	MILLIN	METERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
Α	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
С	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

	MILLIMETERS		INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
D1	6.86	-	0.270	-	
Е	9.65	10.67	0.380	0.420	
E1	6.22	-	0.245	-	
е	2.54 BSC		0.100 BSC		
Н	14.61	15.88	0.575	0.625	
L	1.78	2.79	0.070	0.110	
L1	-	1.65	ı	0.066	
L2	-	1.78	-	0.070	
L3	0.25 BSC		0.010	BSC	
L4	4.78	5.28	0.188	0.208	

ECN: S-82110-Rev. A, 15-Sep-08

DWG: 5970

Notes

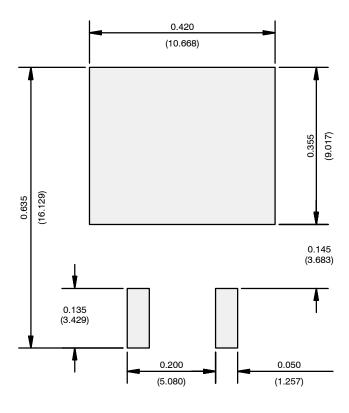
- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- 4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
- 5. Dimension b1 and c1 apply to base metal only.
- 6. Datum A and B to be determined at datum plane H.
- 7. Outline conforms to JEDEC outline to TO-263AB.

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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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