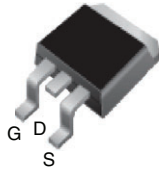


E Series Power MOSFET

D²PAK (TO-263)


N-Channel MOSFET

FEATURES

- 4th generation E series technology
- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low effective capacitance ($C_{o(er)}$)
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V	0.056
Q_g max. (nC)	132	
Q_{gs} (nC)	24	
Q_{gd} (nC)	22	
Configuration	Single	

ORDERING INFORMATION

Package	D ² PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHB065N65E-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	650	V	
Gate-source voltage	V_{GS}	± 30		
Continuous drain current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	40	A
		$T_C = 100$ °C		
Pulsed drain current ^a	I_{DM}	124		
Linear derating factor		2.0	W/°C	
Single pulse avalanche energy ^b	E_{AS}	249	mJ	
Maximum power dissipation	P_D	250	W	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C	
Drain-source voltage slope	dv/dt	$T_J = 125$ °C	100	V/ns
Reverse diode dv/dt ^d		100		
Soldering recommendations (peak temperature) ^c	For 10 s	260	°C	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 120$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 4.2$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $di/dt = 170$ A/ μ s, starting $T_J = 25$ °C



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	62	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	0.5	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		650	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.68	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
		V _{GS} = ± 30 V		-	-	± 1	μA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C		-	-	10	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 15 A	-	0.056	0.065	Ω
Forward transconductance	g _{fs}	V _{DS} = 10 V, I _D = 15 A		-	16	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 100 KHz		-	3500	-	pF
Output capacitance	C _{oss}			-	124	-	
Reverse transfer capacitance	C _{rss}			-	2	-	
Effective output capacitance, energy related	C _{o(er)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		-	135	-	pF
Effective output capacitance, time related	C _{o(tr)}			-	959	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 15 A, V _{DS} = 520 V	-	66	132	nC
Gate-source charge	Q _{gs}			-	24	-	
Gate-drain charge	Q _{gd}			-	22	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 520 V, I _D = 17.3 A, V _{GS} = 10 V, R _g = 10.1 Ω		-	35	70	ns
Rise time	t _r			-	40	80	
Turn-off delay time	t _{d(off)}			-	74	148	
Fall time	t _f			-	13	26	
Gate input resistance	R _g	f = 1 MHz, open drain		0.4	0.9	1.8	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	40	A
Pulsed diode forward current	I _{SM}			-	-	124	
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 15 A, V _{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t _{rr}	T _J = 25 °C, I _F = I _S = 15 A, di/dt = 100 A/μs, V _R = 400 V		-	317	634	ns
Reverse recovery charge	Q _{rr}			-	4.4	8.8	μC
Reverse recovery current	I _{RRM}			-	24	-	A

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

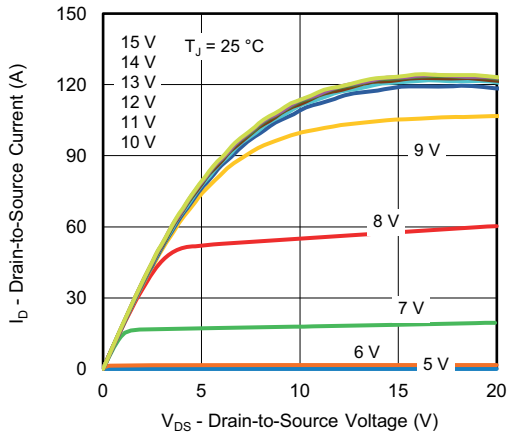


Fig. 1 - Typical Output Characteristics

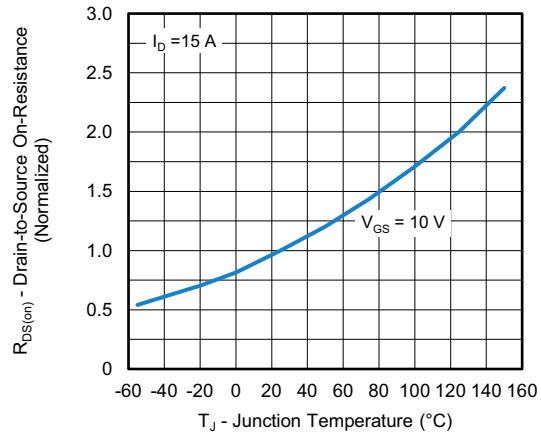


Fig. 4 - Normalized On-Resistance vs. Temperature

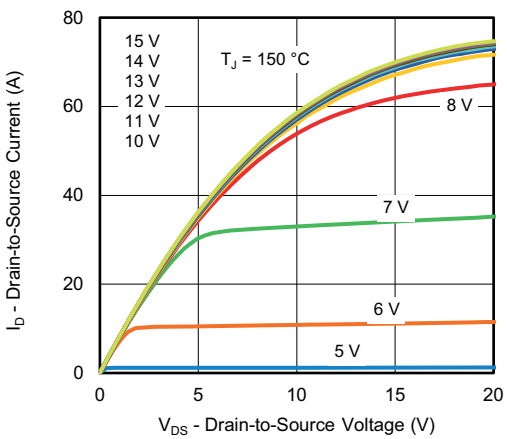


Fig. 2 - Typical Output Characteristics

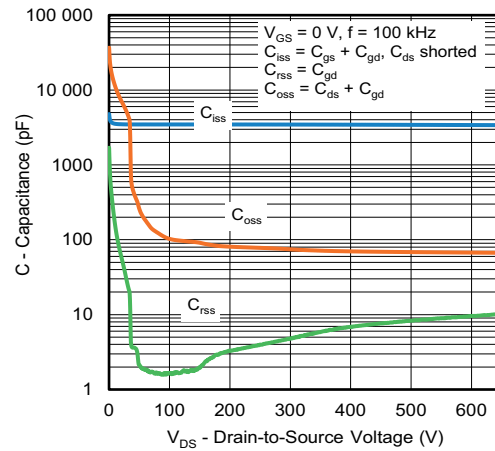


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

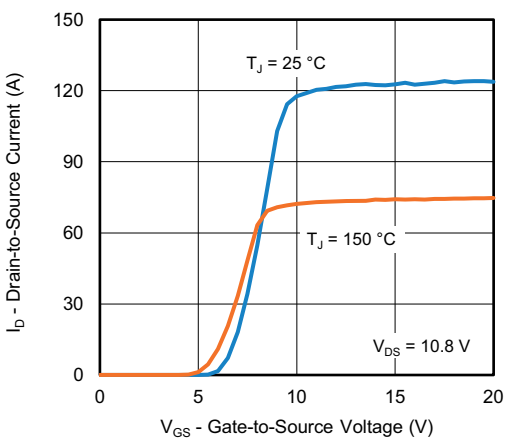


Fig. 3 - Typical Transfer Characteristics

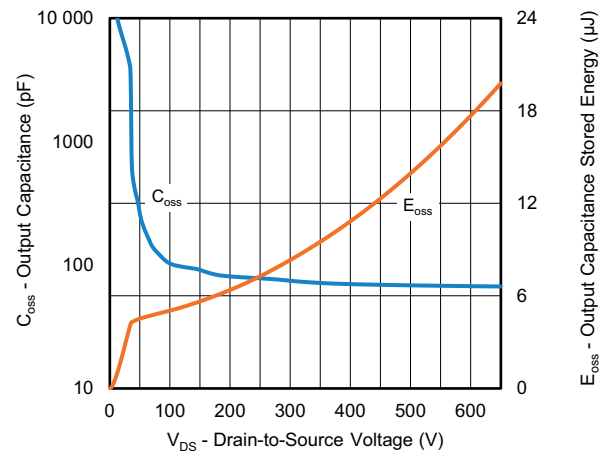


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

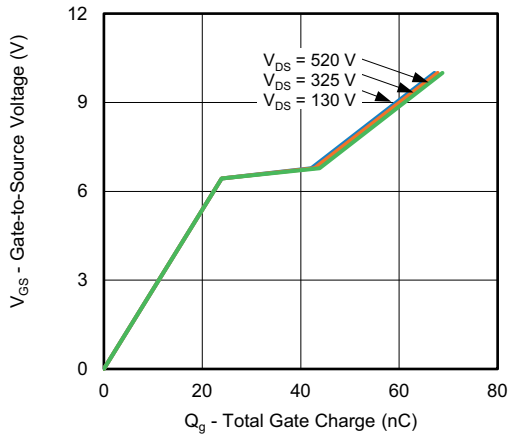


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

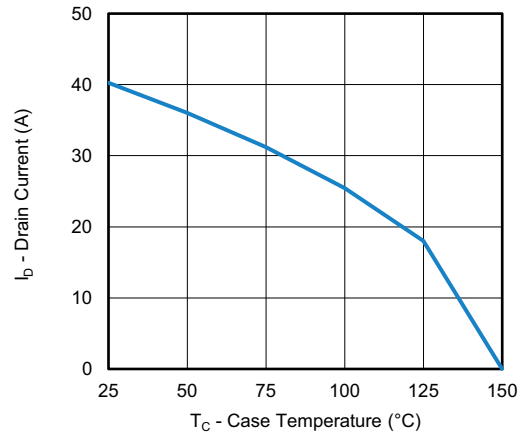


Fig. 9 - Maximum Drain Current vs. Case Temperature

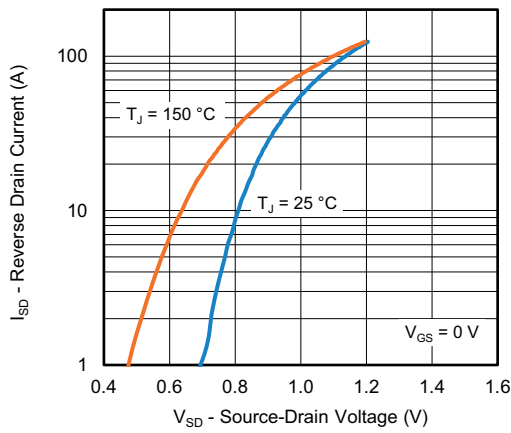


Fig. 8 - Typical Source-Drain Diode Forward Voltage

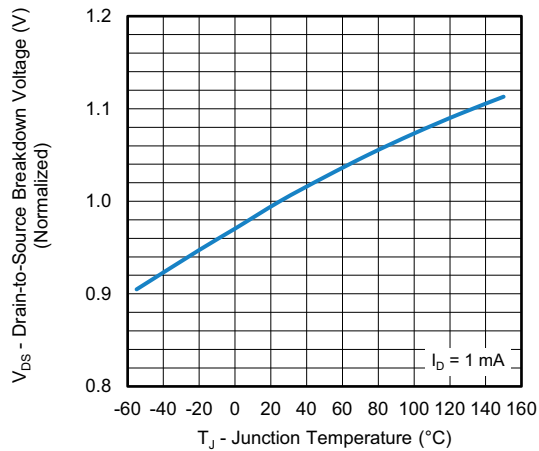


Fig. 10 - Temperature vs. Drain-to-Source Voltage

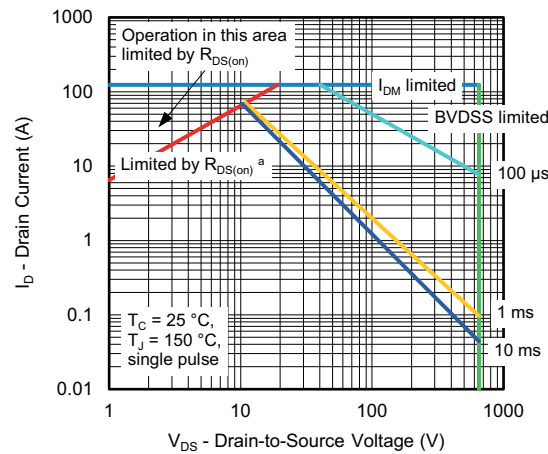


Fig. 11 - Maximum Safe Operating Area

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

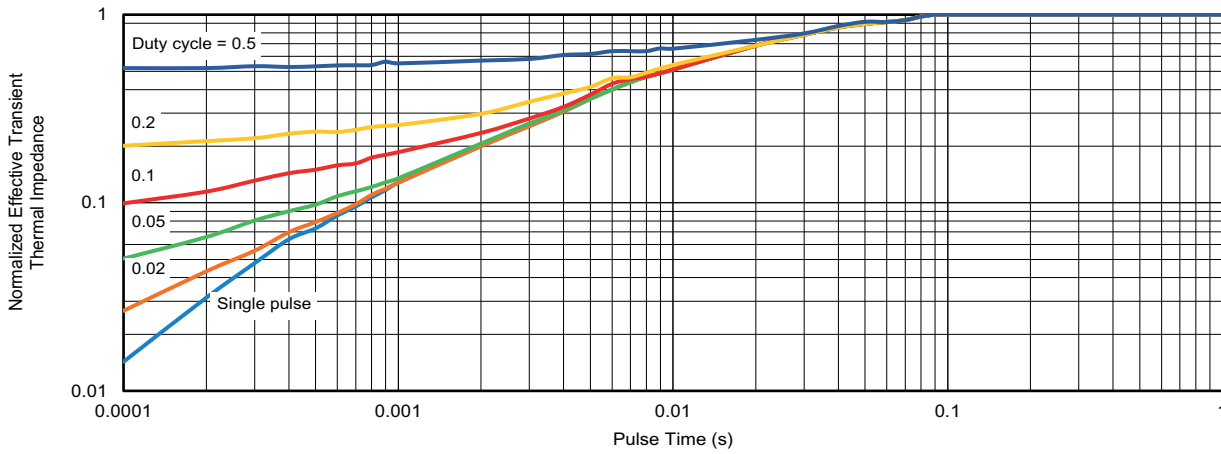


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

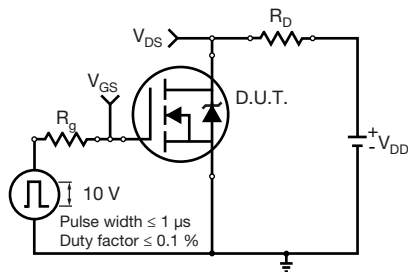


Fig. 13 - Switching Time Test Circuit

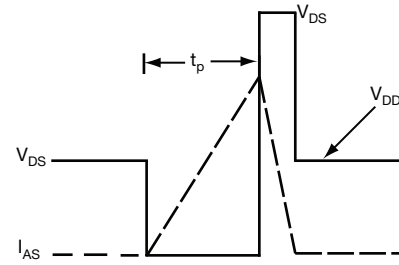


Fig. 16 - Unclamped Inductive Waveforms

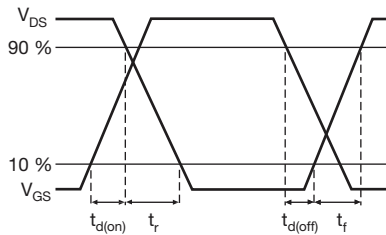


Fig. 14 - Switching Time Waveforms

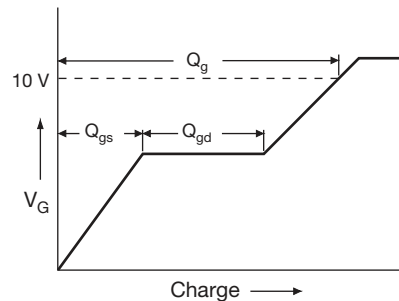


Fig. 17 - Basic Gate Charge Waveform

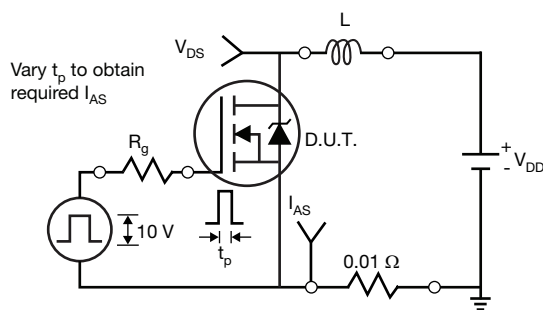


Fig. 15 - Unclamped Inductive Test Circuit

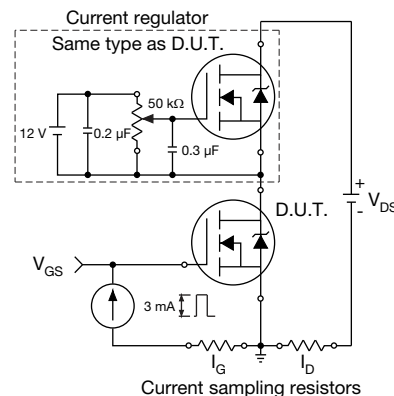
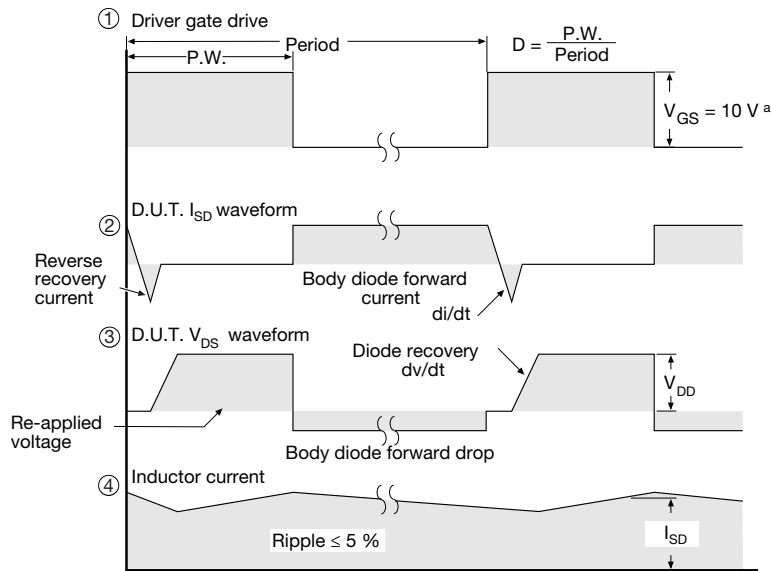
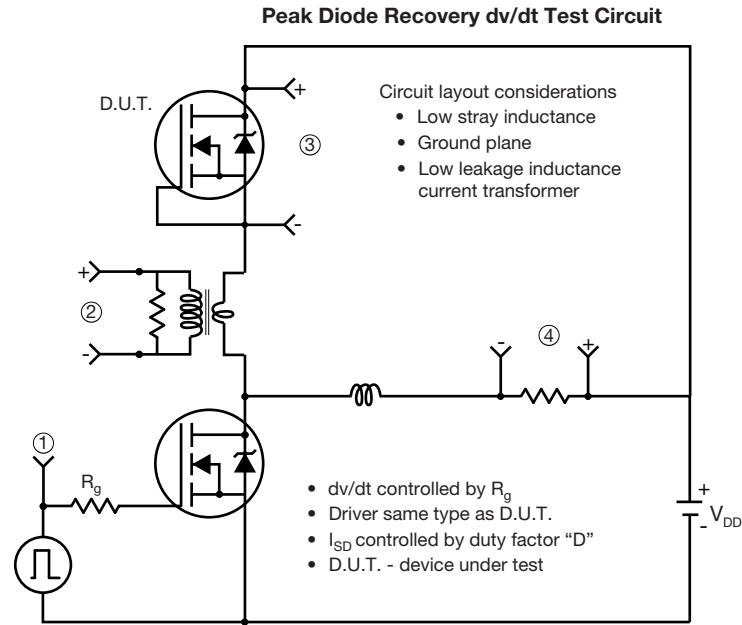


Fig. 18 - Gate Charge Test Circuit



Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 19 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.



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