

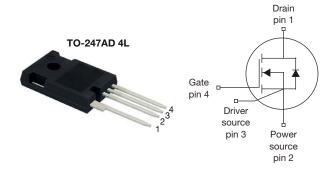
Vishay Siliconix

COMPLIANT

HALOGEN

FREE

E Series Power MOSFET



PRODUCT SUMMARY				
V _{DS} (V) at T _J max.	700			
R _{DS(on)} typ. (Ω) at 25 °C	V _{GS} = 10 V 0.035			
Q _g max. (nC)	138			
Q _{gs} (nC)	36			
Q _{gd} (nC)	27			
Configuration	Single			

FEATURES

- 4th generation E series technology
- Low figure-of-merit (FOM) Ron x Qg
- Low effective capacitance (Co(er))
- · Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- · Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

ORDERING INFORMATION	
Package	TO-247AD 4L
Lead (Pb)-free and halogen-free	SiHL040N65E-GE3

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	650	V
Gate-source voltage			V_{GS}	± 30	v
Continuous drain surrent /T 150 °C)	$T_{\rm C} = 20$		1	65	
Continuous drain current (T _J = 150 °C)	V _{GS} at 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$	· I _D	41	А
Pulsed drain current ^a			I _{DM}	203	
Linear derating factor				3.1	W/°C
Single pulse avalanche energy b			E _{AS}	542	mJ
Maximum power dissipation			P _D	391	W
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C
Drain-source voltage slope		dv/dt	90	1//	
Reverse diode dv/dt ^d			100	- V/ns	
Soldering recommendations (peak temperatur	e) ^c	For 10 s		260	°C

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature
- b. V_{DD} = 120 V, starting T_J = 25 °C, L = 28.2 mH, R_q = 25 Ω , I_{AS} = 6.2 A
- c. 1.6 mm from case
- d. $I_{SD} \le I_D$, di/dt = 200 A/ μ s, starting T_J = 25 °C



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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R _{thJA}	=	40	°C/W	
Maximum junction-to-case (drain)	R_{thJC}	-	0.32	C/VV	

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		650	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = 1 mA	-	0.61	_	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} =	· V _{GS} , I _D = 250 μA	3.0	-	5.0	V
Oala a sanala la la sana	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Gate-source leakage		,	$V_{GS} = \pm 30 \text{ V}$	-	-	± 1	μΑ
Zava gata valtaga dvain avvvant		$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$		-	-	1	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 520 V	, V _{GS} = 0 V, T _J = 125 °C	-	-	10	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 17 A	-	0.035	0.040	Ω
Forward transconductance	9 _{fs}	V _{DS}	= 10 V, I _D = 17 A	-	20	-	S
Dynamic							
Input capacitance	C _{iss}		V _{GS} = 0 V,	-	5344	-	
Output capacitance	C _{oss}		$V_{DS} = 100 \text{ V},$	-	207	-	
Reverse transfer capacitance	C _{rss}		f = 100 KHz		3	-	pF
Effective output capacitance, energy related	C _{o(er)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		-	1510	-	
Effective output capacitance, time related	C _{o(tr)}			-	217	-	
Total gate charge	Qg			-	92	138	
Gate-source charge	Q _{gs}	V _{GS} = 10 V	$I_D = 17 \text{ A}, V_{DS} = 520 \text{ V}$	_	36	-	nC
Gate-drain charge	Q _{gd}				27	-	
Turn-on delay time	t _{d(on)}			-	50	100	
Rise time	t _r	V _{DD} =	V_{DD} = 520 V, I_{D} = 17 A, V_{GS} = 10 V, R_{g} = 10.1 Ω		36	72	
Turn-off delay time	t _{d(off)}	V _{GS} =			105	158	ns
Fall time	t _f				9	18	
Gate input resistance	R_g	f = 1 MHz, open drain		0.4	0.8	1.6	Ω
Drain-Source Body Diode Characteristic	s						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	65	
Pulsed diode forward current	I _{SM}			-	-	203	- A
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 17 A, V _{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t _{rr}	T _J = 25 °C, I _F = I _S = 17 A, di/dt = 100 A/ μ s, V _R = 25 V		-	428	856	ns
Reverse recovery charge	Q _{rr}			-	8	16	μC
Reverse recovery current	I _{RRM}			_	31	-	A



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

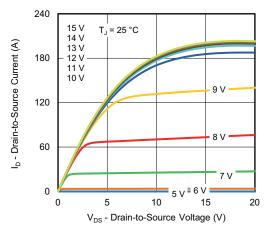


Fig. 1 - Typical Output Characteristics

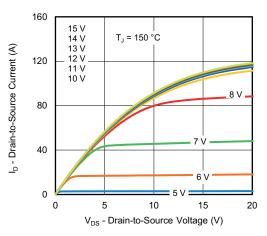


Fig. 2 - Typical Output Characteristics

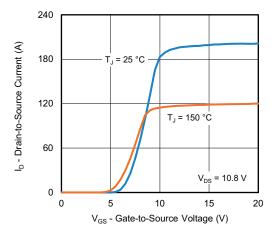


Fig. 3 - Typical Transfer Characteristics

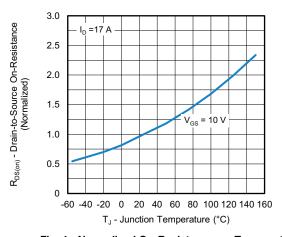


Fig. 4 - Normalized On-Resistance vs. Temperature

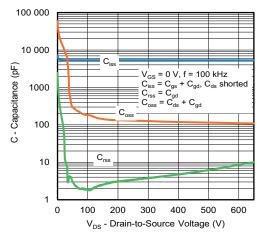


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

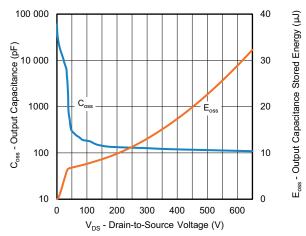


Fig. 6 - Coss and Eoss vs. VDS



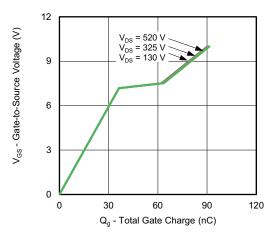


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

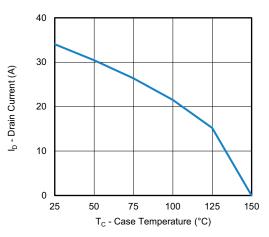


Fig. 9 - Maximum Drain Current vs. Case Temperature

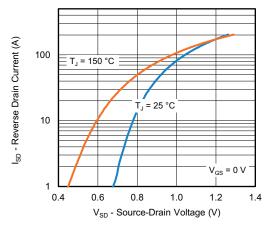


Fig. 8 - Typical Source-Drain Diode Forward Voltage

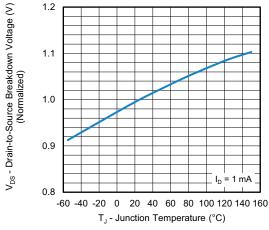


Fig. 10 - Temperature vs. Drain-to-Source Voltage

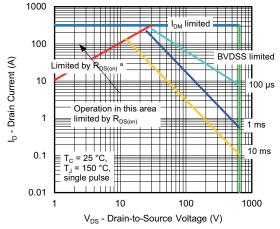


Fig. 11 - Maximum Safe Operating Area

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



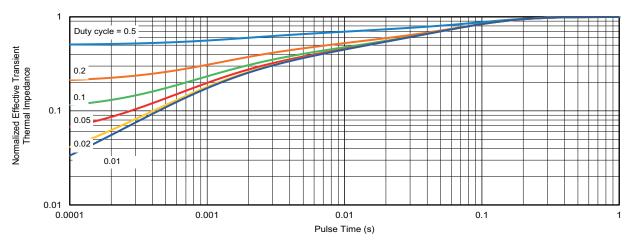


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

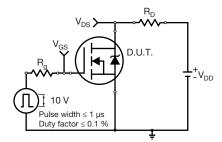


Fig. 13 - Switching Time Test Circuit

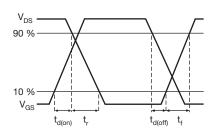


Fig. 14 - Switching Time Waveforms

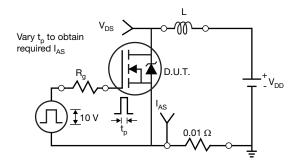


Fig. 15 - Unclamped Inductive Test Circuit

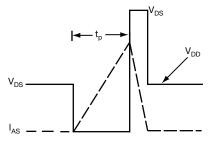


Fig. 16 - Unclamped Inductive Waveforms

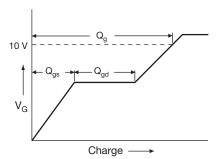


Fig. 17 - Basic Gate Charge Waveform

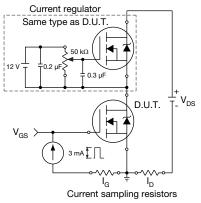
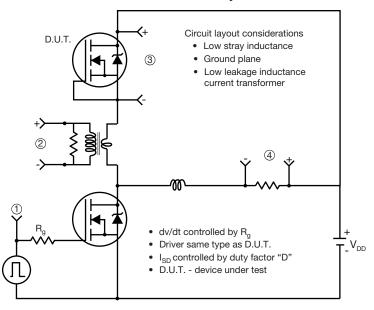


Fig. 18 - Gate Charge Test Circuit



Peak Diode Recovery dv/dt Test Circuit



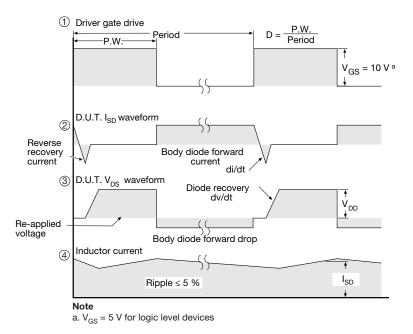


Fig. 19 - For N-Channel

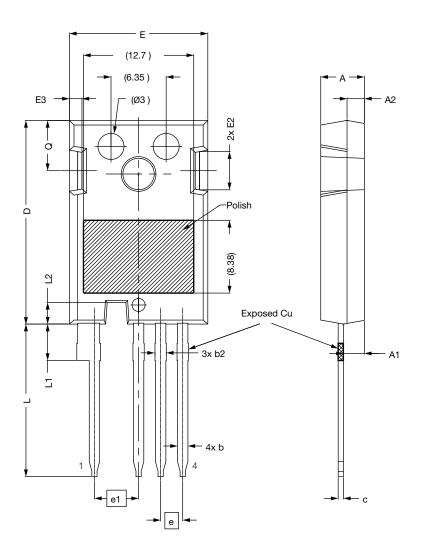
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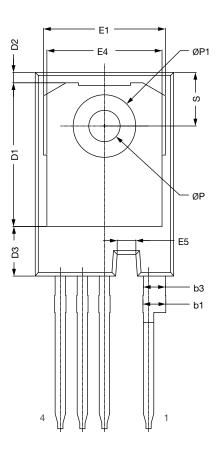


Vishay MaxPower Semiconductor

Case Outline for TO-247AD 4L Package

FACILITY CODE: 9







Package Information

www.vishay.com

Vishay MaxPower Semiconductor

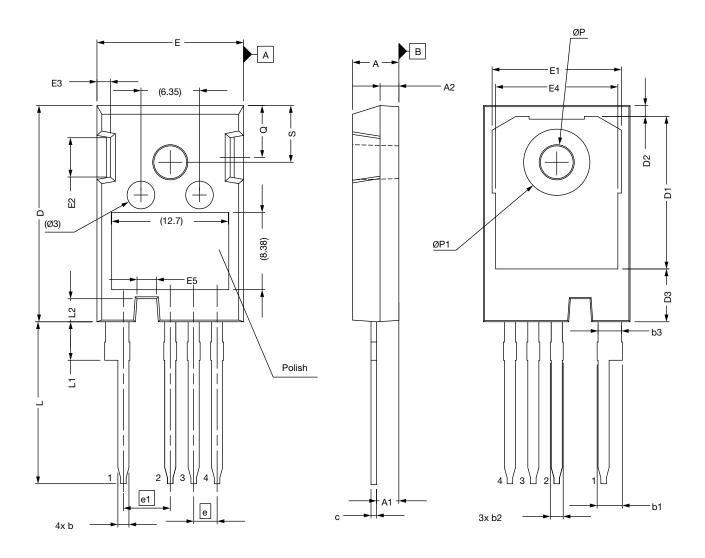
DIM.	MILLIMETERS		
DIWI.	MIN.	MAX.	
A	4.83	5.21	
A1	2.29	2.54	
A2	1.91	2.16	
b	1.07	1.33	
b1	2.39	2.94	
b3	1.07	1.60	
С	0.55	0.68	
D	23.30	23.60	
D1	16.25	17.65	
D2	0.95	1.25	
E	15.75	16.13	
E1	13.10	14.15	
E2	3.68	5.10	
E3	1.00	1.90	
E4	12.38	13.43	
E5	1.95	2.35	
e	2.54 E	BSC.	
e1	5.08 BSC.		
L	17.31	17.82	
L1	3.97	4.37	
L2	2.35	2.65	
ØP	3.51	3.65	
Q	5.49	6.00	
S	6.04	6.30	

Notes

- All dimensions are in mm. Angles are in degrees
- Dimension D and E do not include mold flash
- All metal surfaces: tin plated, except area of cut
- Dimensioning and toleranceing confirm to ASME Y14.5M-1994
- Creepage 1 is 8.58 mm (ref.) which is the distance alongside the surface between drain (pin 1) and trough the notch towards source (pin 2). Creepage 2 is 7.95 mm (ref.) which is the distance from end of the copper slug on the backside of the package to either pin 2, pin 3 or pin 4

Vishay MaxPower Semiconductor

FACILITY CODE: N





Package Information

www.vishay.com

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DIM.		MILLIMETERS				
DIM.	MIN.	NOM.	MAX.			
Α	4.83	5.02	5.21			
A1	2.29	2.41	2.54			
A2	1.91	2.00	2.16			
b	1.07	1.20	1.33			
b1	2.39	2.67	2.94			
b2	1.07	1.30	1.60			
b3	2.39	2.53	2.69			
С	0.55	0.60	0.68			
D	23.30	23.45	23.60			
D1	16.25	16.55	17.65			
D2	0.95	1.19	1.25			
D3	5.55	5.71	6.01			
Е	15.75	15.94	16.13			
E1	13.10	14.02	14.15			
E2	3.68	4.40	5.10			
E3	1.00	1.45	1.90			
E4	12.38	13.26	13.43			
E5	1.95	2.15	2.35			
е		2.54 BSC.				
e1		5.08 BSC.				
L	17.31	17.57	17.82			
L1	3.97	4.19	4.37			
L2	2.35	2.50	2.65			
ØP	3.51	3.61	3.65			
ØP1	7.19 ref.					
Q	5.49	5.79	6.00			
S	6.04	6.17	6.30			
FCN: \$25-0851-Rev. C. 18-Jul-202	- 5	1				

ECN: S25-0851-Rev. C, 18-Jul-2025

DWG: 6121

Notes

- All dimensions are in mm
- Dimension D and E do not include mold flash.
- Creepage 1 is 8.40 mm (ref.) which is the distance alongside the surface between drain (pin 1) and trough the notch towards source (pin 2). Creepage 2 is 7.70 mm (ref.) which is the distance from end of the copper slug on the backside of the package to either pin 2, pin 3 or pin 4



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