

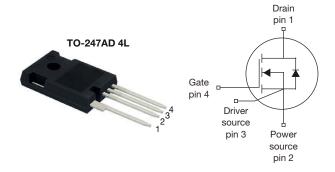
Vishay Siliconix

COMPLIANT

HALOGEN

FREE

E Series Power MOSFET



PRODUCT SUMMARY					
V _{DS} (V) at T _J max.	700				
R _{DS(on)} typ. (Ω) at 25 °C	$V_{GS} = 10 \text{ V}$	0.023			
Q _g max. (nC)	236				
Q _{gs} (nC)	67				
Q _{gd} (nC)	49				
Configuration	Single				

FEATURES

- 4th generation E series technology
- Low figure-of-merit (FOM) R_{on} x Q_g
- Low effective capacitance (Co(er))
- · Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

ORDERING INFORMATION	
Package	TO-247AD 4L
Lead (Pb)-free and halogen-free	SiHL026N65E-GE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V_{DS}	650		
Gate-source voltage			V_{GS}	± 30	V	
Continuous drain current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 25 °C	I _D	88	А	
	VGS at 10 V	T _C = 100 °C		55		
Pulsed drain current ^a			I _{DM}	323	1	
Linear derating factor				3.7	W/°C	
Single pulse avalanche energy b			E _{AS}	948	mJ	
Maximum power dissipation			P_{D}	179	W	
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C	
Drain-source voltage slope		-l / -l.	100	\//n -		
Reverse diode dv/dt c			dv/dt 10		V/ns	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature
- b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω , I_{AS} = 8.2 A
- c. $I_{SD} \le I_D$, di/dt = 100 A/ μ s, starting $T_J = 25$ °C



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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R _{thJA}	-	40	°C/W	
Maximum junction-to-case (drain)	R _{thJC}	-	0.27	C/ VV	

PARAMETER	SYMBOL	TES	TEST CONDITIONS		TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		650	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Referenc	Reference to 25 °C, I _D = 1 mA		0.63	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} =	· V _{GS} , I _D = 250 μA	3.0	-	5.0	V
	I _{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Gate-source leakage		,	$V_{GS} = \pm 30 \text{ V}$	-	-	± 1	μΑ
		V _{DS} =	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$		-	1	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 520 V	V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C		-	10	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 40 A	-	0.023	0.026	Ω
Forward transconductance a	9 _{fs}	V _{DS} = 10 V, I _D = 40 A		-	35	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V,		-	9286	-	pF
Output capacitance	C _{oss}	,	V _{BS} = 0 V, V _{DS} = 100 V,		284	-	
Reverse transfer capacitance	C _{rss}	f = 100 kHz		-	6	-	
Effective output capacitance, energy related ^a	C _{o(er)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		-	353	-	
Effective output capacitance, time related ^b	C _{o(tr)}			-	2481	-	
Total gate charge	Qg			-	157	236	
Gate-source charge	Q _{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 40 \text{ A}, V_{DS} = 520 \text{ V}$		67	-	nC
Gate-drain charge	Q _{gd}				49	-	
Turn-on delay time	t _{d(on)}		$V_{DD} = 520 \text{ V}, I_D = 40 \text{ A}, V_{GS} = 10 \text{ V}, R_g = 10.1 \Omega$		101	152	
Rise time	t _r	V _{DD} =			100	150	
Turn-off delay time	t _{d(off)}				142	213	ns
Fall time	t _f	1		-	31	62	
Gate input resistance	R_g	f = 1 MHz, open drain		0.4	0.9	1.8	Ω
Drain-Source Body Diode Characteristic	s						
Continuous source-drain diode current	Is	MOSFET sym showing the	MOSFET symbol showing the		-	88	
Pulsed diode forward current	I _{SM}	integral reverse p - n junction diode		-	-	323	A
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 40 A, V _{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t _{rr}	$T_J = 25 \text{ °C}, I_F = I_S = 40 \text{ A},$ $di/dt = 100 \text{ A/}\mu\text{s}, V_R = 25 \text{ V}$		-	594	1188	ns
Reverse recovery charge	Q _{rr}			-	15	30	μC
Reverse recovery current	I _{RRM}			_	42	-	Α



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

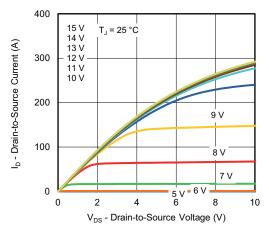


Fig. 1 - Typical Output Characteristics

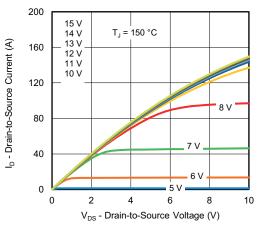


Fig. 2 - Typical Output Characteristics

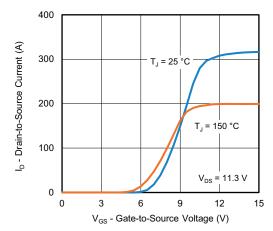


Fig. 3 - Typical Transfer Characteristics

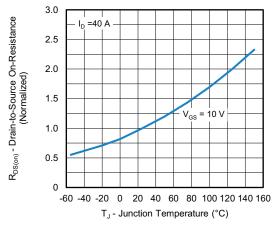


Fig. 4 - Normalized On-Resistance vs. Temperature

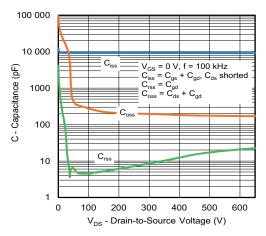


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

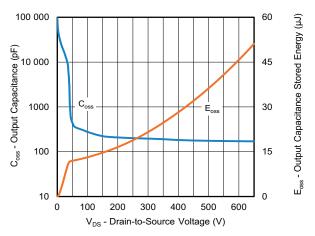


Fig. 6 - Coss and Eoss vs. VDS



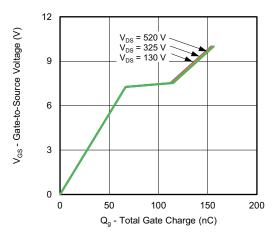


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

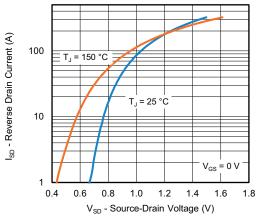


Fig. 8 - Typical Source-Drain Diode Forward Voltage

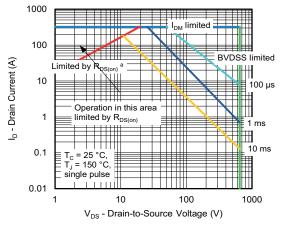


Fig. 9 - Maximum Safe Operating Area

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

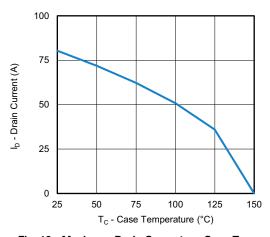


Fig. 10 - Maximum Drain Current vs. Case Temperature

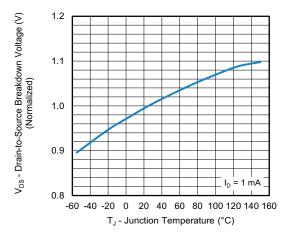


Fig. 11 - Temperature vs. Drain-to-Source Voltage



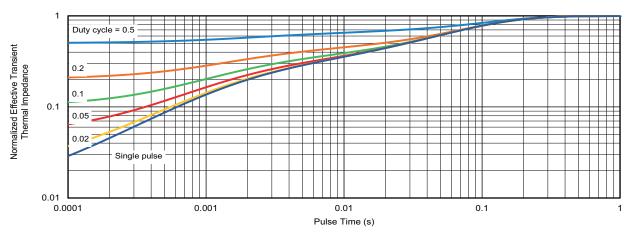


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

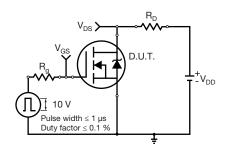


Fig. 13 - Switching Time Test Circuit

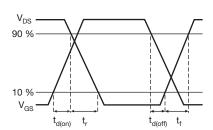


Fig. 14 - Switching Time Waveforms

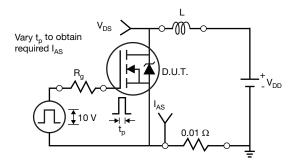


Fig. 15 - Unclamped Inductive Test Circuit

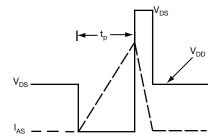


Fig. 16 - Unclamped Inductive Waveforms

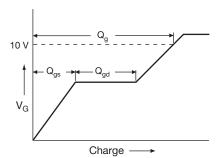


Fig. 17 - Basic Gate Charge Waveform

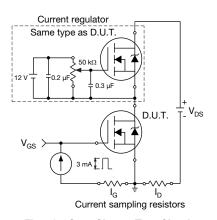
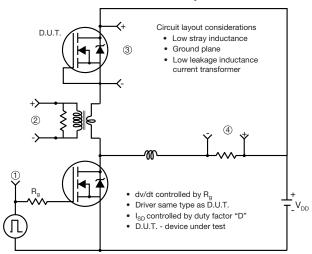


Fig. 18 - Gate Charge Test Circuit



Peak Diode Recovery dv/dt Test Circuit



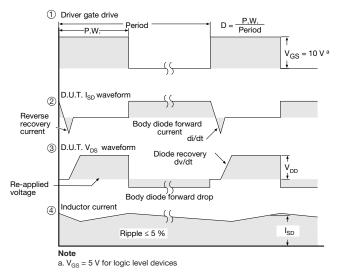


Fig. 19 - For N-Channel

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