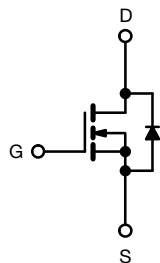
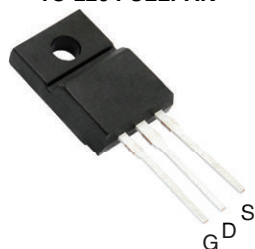


S Series Power MOSFET

TO-220 FULLPAK


N-Channel MOSFET

FEATURES

- Latest generation SF series technology
- Low figure of merit (FOM) $R_{DS(on)} \times Q_g$
- Low effective capacitance ($C_{o(er)}$)
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V	0.121
Q_g max. (nC)	77	
Q_{gs} (nC)	13	
Q_{gd} (nC)	26	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free and halogen-free	SiHF135N65S-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V _{DS}	650	V
Gate-source voltage			V _{GS}	± 20	
Continuous drain current (T _J = 150 °C) ^d	V _{GS} at 10 V	T _C = 25 °C	I _D	10	A
		T _C = 100 °C		6	
Pulsed drain current ^a			I _{DM}	62	
Linear derating factor				0.28	W/°C
Single pulse avalanche energy ^b			E _{AS}	298	mJ
Maximum power dissipation			P _D	35	W
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C
Drain-source voltage slope		T _J = 125 °C	dv/dt	100	V/ns
Reverse diode dv/dt ^c				100	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 120$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 4.6$ A
- $I_{SD} \leq I_D$, di/dt = 850 A/ μ s, starting $T_J = 25$ °C
- Limited by maximum junction temperature

**THERMAL RESISTANCE RATINGS**

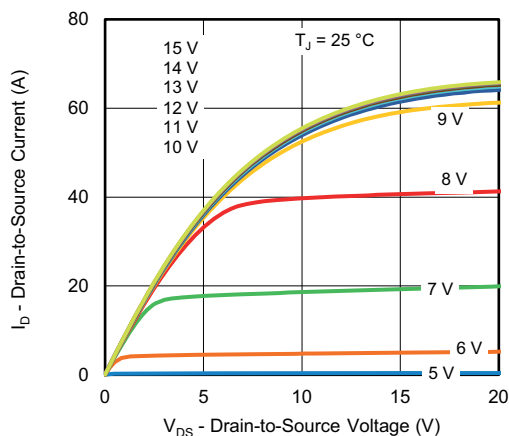
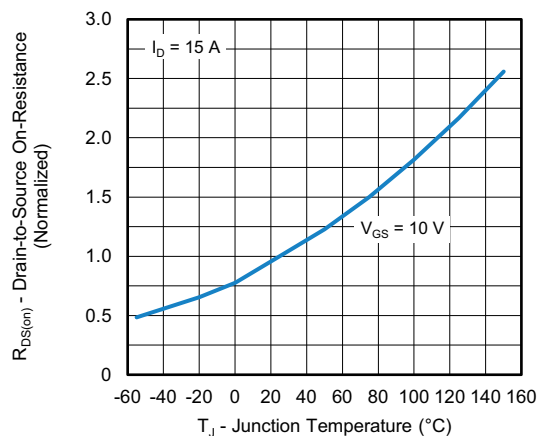
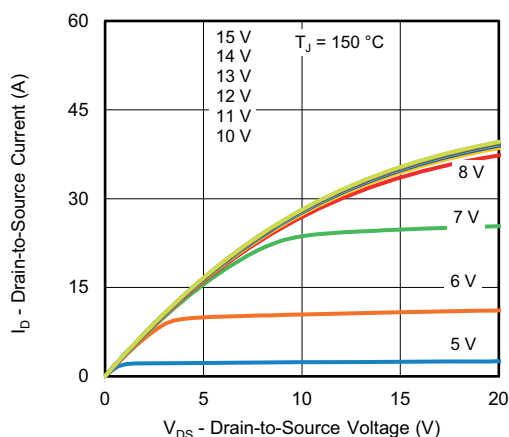
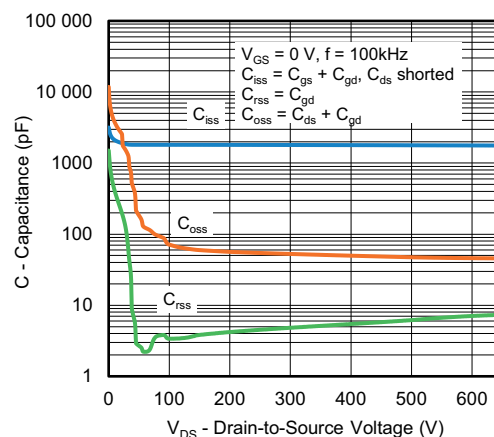
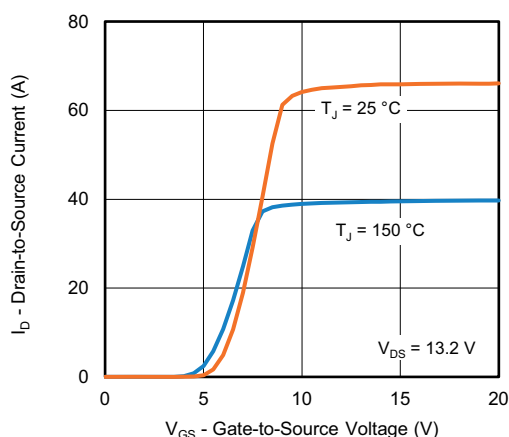
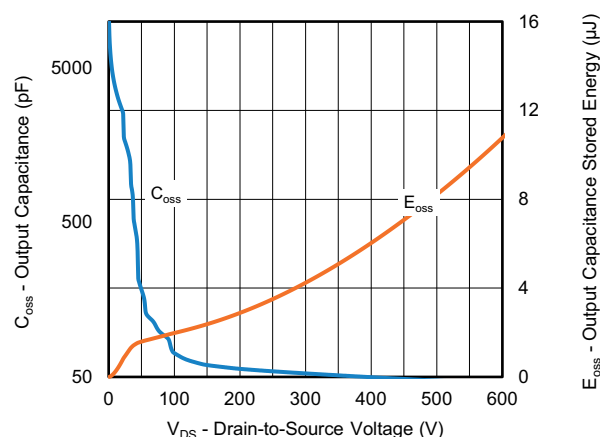
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	65	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	3.6	

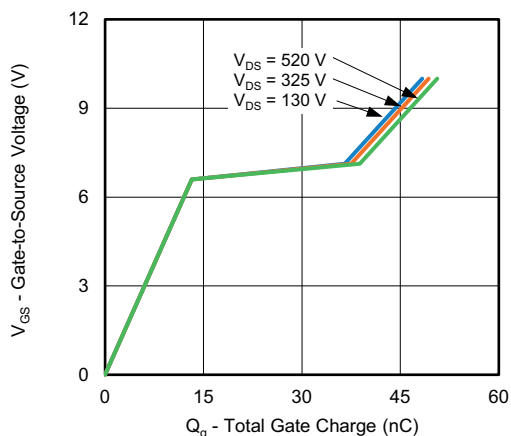
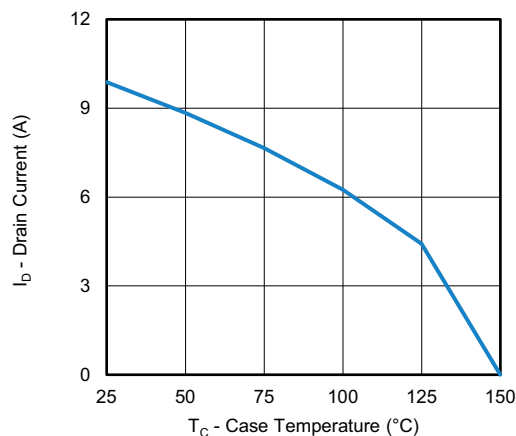
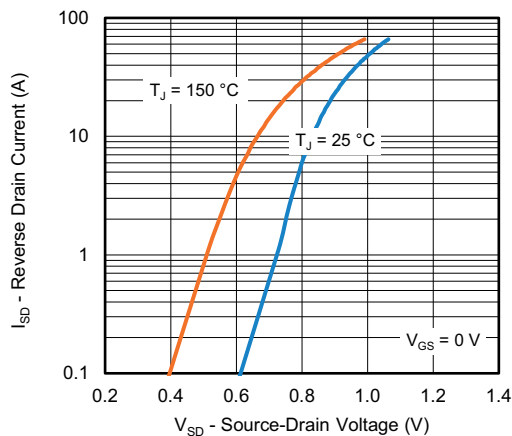
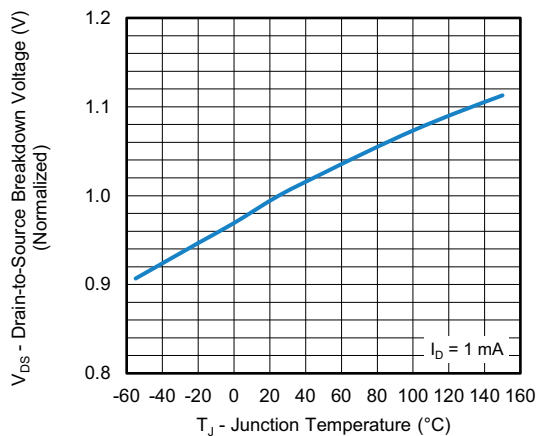
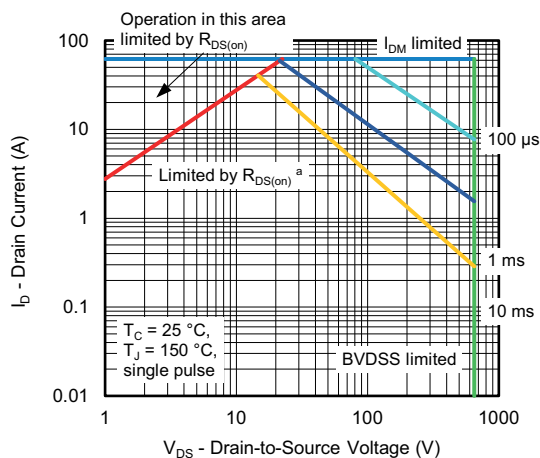
SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		650	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.63	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C		-	-	2	mA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 15 A	-	0.121	0.139	Ω
Forward transconductance ^a	g _{fs}	V _{DS} = 20 V, I _D = 15 A		-	12	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 100 KHz		-	1808	-	pF
Output capacitance	C _{oss}			-	92	-	
Reverse transfer capacitance	C _{rss}			-	3	-	
Effective output capacitance, energy related ^a	C _{o(er)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		-	75	-	
Effective output capacitance, time related ^b	C _{o(tr)}			-	348	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 15 A, V _{DS} = 520 V	-	51	77	nC
Gate-source charge	Q _{gs}			-	13	-	
Gate-drain charge	Q _{gd}			-	26	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 520 V, I _D = 17.5 A, V _{GS} = 10 V, R _g = 10.1 Ω		-	20	40	ns
Rise time	t _r			-	36	72	
Turn-off delay time	t _{d(off)}			-	60	90	
Fall time	t _f			-	19	38	
Gate input resistance	R _g	f = 1 MHz, open drain		0.5	1.0	2.0	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	27	A
Pulsed diode forward current	I _{SM}			-	-	62	
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 15 A, V _{GS} = 0 V		-	-	1.4	V
Reverse recovery time	t _{rr}	T _J = 25 °C, I _F = I _S = 15 A, di/dt = 100 A/μs, V _R = 25 V		-	347	694	ns
Reverse recovery charge	Q _{rr}			-	5.7	11.4	μC
Reverse recovery current	I _{RRM}			-	32	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 V to 400 V
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to 400 V

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Typical Source-Drain Diode Forward Voltage

Fig. 11 - Temperature vs. Drain-to-Source Voltage

Fig. 9 - Maximum Safe Operating Area
Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

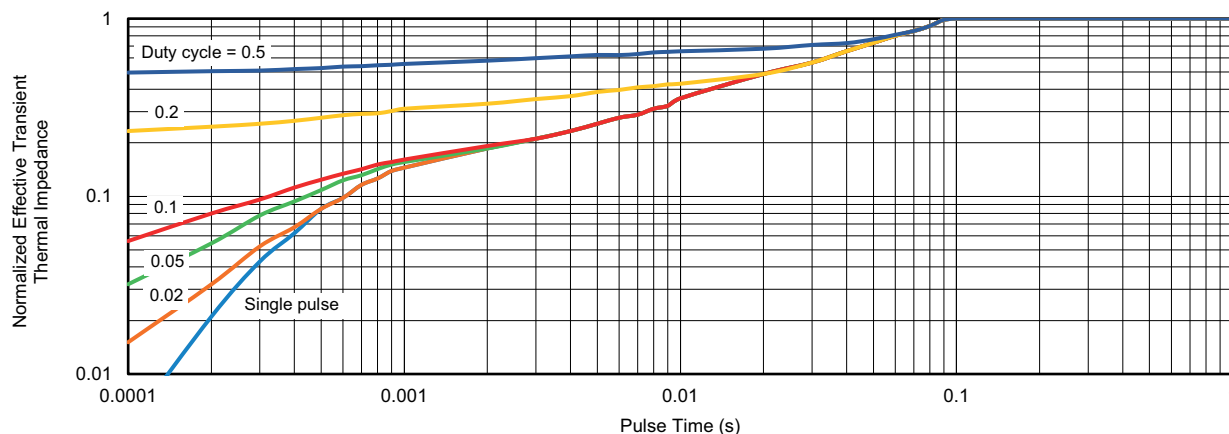


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

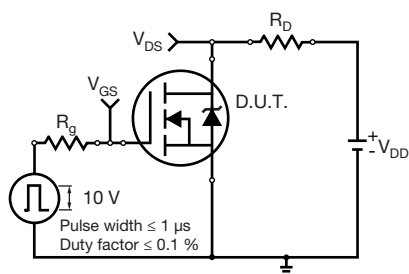


Fig. 13 - Switching Time Test Circuit

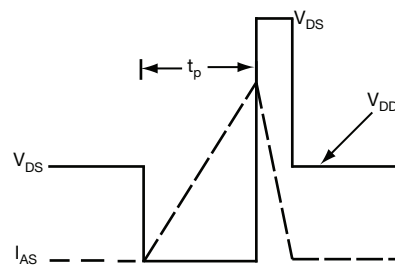


Fig. 16 - Unclamped Inductive Waveforms

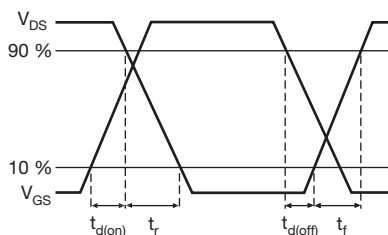


Fig. 14 - Switching Time Waveforms

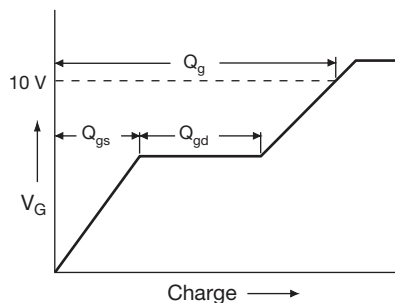


Fig. 17 - Basic Gate Charge Waveform

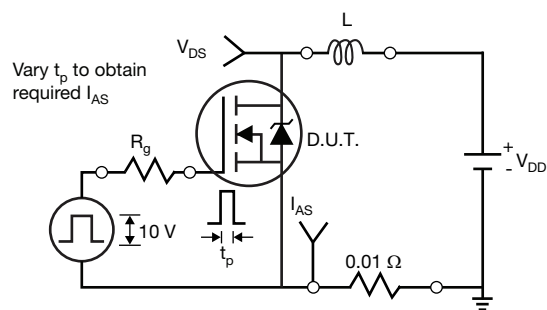


Fig. 15 - Unclamped Inductive Test Circuit

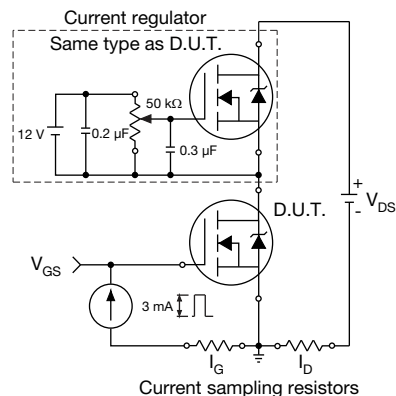


Fig. 18 - Gate Charge Test Circuit

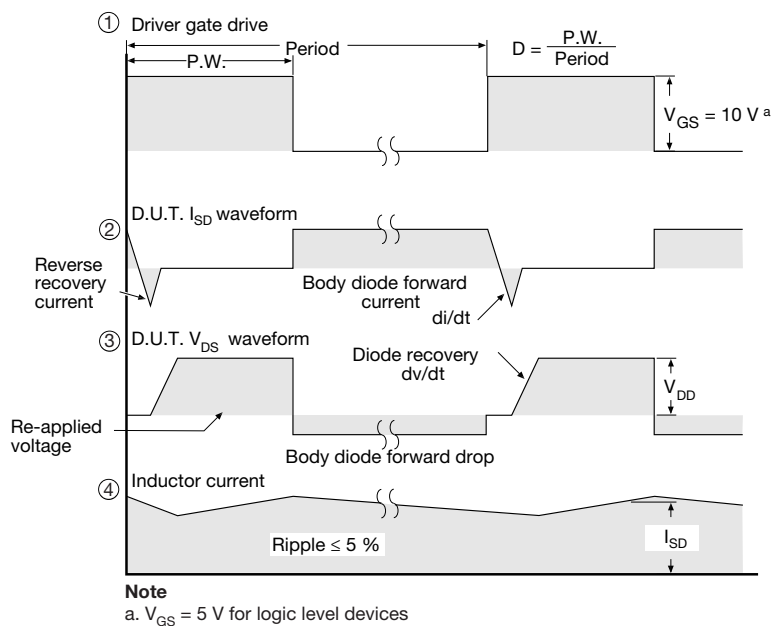


Fig. 19 - For N-Channel

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