# VS-VSK.230...PbF Series

**Vishay Semiconductors** 

### SCR/SCR and SCR/Diode (MAGN-A-PAK Power Modules), 230 A



www.vishay.com

**MAGN-A-PAK** 

230 A

Modules - thyristor, standard

MAGN-A-PAK

**PRIMARY CHARACTERISTICS** 

I<sub>T(AV)</sub>

Type

Package

# **FEATURES**

- High voltage
- · Electrically isolated base plate
- 3500 V<sub>RMS</sub> isolating voltage
- Industrial standard package
- · Simplified mechanical designs, rapid assembly
- · High surge capability
- Large creepage distances
- UL approved file E78996
- · Designed and qualified for industrial level
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

#### DESCRIPTION

This VSK series of MAGN-A-PAK modules uses high voltage power thyristor/thyristor and thyristor/diode in seven basic configurations. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built. They can be interconnected to form single phase or three phase bridges or as AC-switches when modules are connected in anti-parallel mode. These modules are intended for general purpose applications such as battery chargers, welders, motor drives, UPS, etc.

MAJOR RATINGS AND CHARACTERISTICS						
SYMBOL	CHARACTERISTICS	VALUES	UNITS			
I <sub>T(AV)</sub>	85 °C	230				
I <sub>T(RMS)</sub>		510	Α			
ITSM	50 Hz	7500	A			
	60 Hz	7850				
l <sup>2</sup> t	50 Hz	280	kA <sup>2</sup> s			
	60 Hz	260	KA-S			
l²√t		280	kA²√s			
V <sub>DRM</sub> /V <sub>RRM</sub>		800 to 2000	V			
TJ	Range	-40 to +130	°C			

#### **ELECTRICAL SPECIFICATIONS**

VOLTAGE RATINGS								
TYPE NUMBER	VOLTAGE CODE	V <sub>RRM</sub> /V <sub>DRM</sub> , MAXIMUM REPETITIVE PEAK REVERSE AND OFF-STATE BLOCKING VOLTAGE V	V <sub>RSM</sub> , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I <sub>RRM</sub> /I <sub>DRM</sub> AT 130 °C MAXIMUM mA				
	08	800	900					
	12	1200	1300					
VS-VSK.230-	16	1600	1700	50				
	18	1800	1900					
	20	2000	2100					

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<b>ON-STATE CONDUCTION</b>						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current	I <sub>T(AV)</sub>	180° conductio	on, half sine wave		230	А
at case temperature			n, nan sine wave		85	°C
Maximum RMS on-state current	I <sub>T(RMS)</sub>	As AC switch			510	
		t = 10 ms	No voltage		7500	
Maximum peak, one-cycle on-state		t = 8.3 ms	reapplied		7850	А
non-repetitive, surge current	I <sub>TSM</sub>	t = 10 ms	100 % V <sub>RRM</sub>	Sinusoidal	6300	- kA <sup>2</sup> s
		t = 8.3 ms	reapplied	half wave,	6600	
		t = 10 ms	No voltage	initial $T_J = T_J$ maximum	280	
Maximum I <sup>2</sup> t for fusing	l <sup>2</sup> t	t = 8.3 ms	reapplied		256	
Maximum i-t for fusing	1-1	t = 10 ms	100 % V <sub>RRM</sub>		198	
		t = 8.3 ms	reapplied		181	
Maximum I <sup>2</sup> √t for fusing	l²√t	t = 0.1 ms to 1	0 ms, no voltage	reapplied	2800	kA²√s
Low level value or threshold voltage	V <sub>T(TO)1</sub>	(16.7 % x π x I-	<sub>T(AV)</sub> < I < π x I <sub>T(AV</sub>	), T <sub>J</sub> = T <sub>J</sub> maximum	1.03	V
High level value of threshold voltage	V <sub>T(TO)2</sub>	$(I > \pi \times I_{T(AV)}), T$	$J = T_J$ maximum		1.07	v
Low level value on-state slope resistance	r <sub>t1</sub>	(16.7 % x π x I-	<sub>T(AV)</sub> < I < π x I <sub>T(AV</sub>	), T <sub>J</sub> = T <sub>J</sub> maximum	0.77	mΩ
High level value on-state slope resistance	r <sub>t2</sub>	$(I > \pi \times I_{T(AV)}), T$	$J = T_J$ maximum		0.73	1115.2
Maximum on-state voltage drop	V <sub>TM</sub>	$ \begin{split} I_{TM} &= \pi \; x \; I_{T(AV)}, \; T_J = T_J \; maximum, \; 180^\circ \; conduction, \\ average \; power = V_{T(TO)} \; x \; I_{T(AV)} + r_f \; x \; (I_{T(RMS)})^2 \end{split} $			1.59	V
Maximum holding current	Ι <sub>Η</sub>	Anode supply = 12 V, initial $I_T$ = 30 A, $T_J$ = 25 °C		500		
Maximum latching current	١L		y = 12 V, resis V, 100 μs, T <sub>J</sub> = 2	stive load = 1 Ω, 5 °C	1000	mA

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Typical delay time	t <sub>d</sub>	$T_J = 25$ °C, gate current = 1 A dl <sub>q</sub> /dt = 1 A/µs,	1.0	
Typical rise time	t <sub>r</sub>	$V_{d} = 0.67 \% V_{DRM}$	2.0	μs
Typical turn-off time	tq	$I_{TM}$ = 300 A; dl/dt = 15 A/μs; T <sub>J</sub> = T <sub>J</sub> maximum; V <sub>R</sub> = 50 V; dV/dt = 20 V/μs; gate 0 V, 100 Ω	50 to 150	μο

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse and off-state leakage current	I <sub>RRM,</sub> I <sub>DRM</sub>	$T_J = T_J maximum$	50	mA
RMS insulation voltage	V <sub>INS</sub>	50 Hz, circuit to base, all terminals shorted, 25 $^\circ\text{C},$ 1 s	3000	V
Critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, exponential to 67 % rated $V_{DRM}$	1000	V/µs

TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak gate power	P <sub>GM</sub>	$t_p \le 5 \text{ ms}, T_J = T_J \text{ max}$	imum	10.0	W
Maximum average gate power	P <sub>G(AV)</sub>	$f = 50 Hz, T_J = T_J max$	imum	2.0	vv
Maximum peak gate current	+ I <sub>GM</sub>	$t_p \le 5 \text{ ms}, T_J = T_J \text{ max}$	imum	3.0	А
Maximum peak negative gate voltage	- V <sub>GT</sub>	$t_p \le 5 \text{ ms}, T_J = T_J \text{ max}$	imum	5.0	
		T <sub>J</sub> = -40 °C	Anode supply = 12 V, resistive load; Ra = 1 $\Omega$	4.0	V
Maximum required DC gate voltage to trigger	V <sub>GT</sub>	T <sub>J</sub> = 25 °C		3.0	
		$T_J = T_J maximum$		2.0	
		T <sub>J</sub> = - 40 °C		350	
Maximum required DC gate current to trigger	I <sub>GT</sub>	T <sub>J</sub> = 25 °C	Anode supply = 12 V, resistive load; Ra = 1 $\Omega$	200	mA
		$T_J = T_J maximum$		100	
Maximum gate voltage that will not trigger	V <sub>GD</sub>	$T_J = T_J$ maximum, rated $V_{DRM}$ applied		0.25	V
Maximum gate current that will not trigger	I <sub>GD</sub>	$T_J = T_J$ maximum, rate	ed V <sub>DRM</sub> applied	10.0	mA
Maximum rate of rise of turned-on current	dl/dt	$T_J = T_J$ maximum, $I_{TM}$	= 400 A, rated $V_{DRM}$ applied	500	A∕µs

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THERMAL AND MECHANICAL SPECIFICATIONS							
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS		
Junction operatin	ng temperature range	TJ		-40 to +130	°C		
Storage temperat	ture range	T <sub>Stg</sub>		-40 to +150	U		
Maximum thermal resistance, junction to case per junction		R <sub>thJC</sub>	DC operation	0.125	K/W		
Typical thermal resistance, case to heatsink per module		R <sub>thCS</sub>	Mounting surface flat, smooth, and greased	0.02	r∨ vv		
Mounting	MAGN-A-PAK to heatsink		A mounting compound is recommended and the torgue should be rechecked after a period	414.0	Nu		
torque ± 10 %	busbar to MAGN-A-PAK		of about 3 h to allow for the spread of the compound.	4 to 6	Nm		
Approximate weight				500	g		
	grit			17.8	oz.		
Case style				MAGN-A	-PAK		

DEVICES	SINUSOIDAL CONDUCTION AT TJ MAXIMUM					RECTANGULAR CONDUCTION AT T <sub>J</sub> MAXIMUM					UNITS
DEVICES	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VSK.230-	0.009	0.010	0.010	0.020	0.032	0.007	0.011	0.015	0.020	0.033	K/W

#### Note

• Table shows the increment of thermal resistance R<sub>thJC</sub> when devices operate at different conduction angles than DC

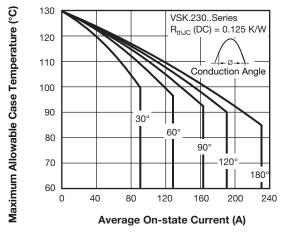


Fig. 1 - Current Ratings Characteristics

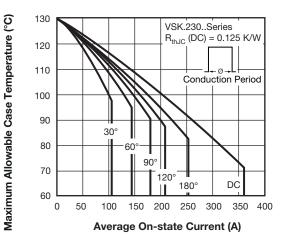


Fig. 2 - Current Ratings Characteristics



#### 350 180° Maximum Average On-State Power Loss (W) 120° 300 90 60° 250 30° 200 RMS limit 150 Conduction Angle 100 VSK.230..Series Per Junction 50 T<sub>J</sub> = 130 °C 0 200 0 50 100 150 250 Average On-state Current (A)

Fig. 3 - On-State Power Loss Characteristics

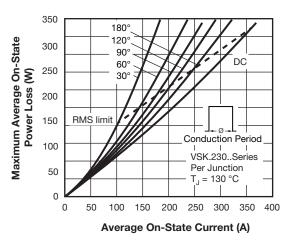
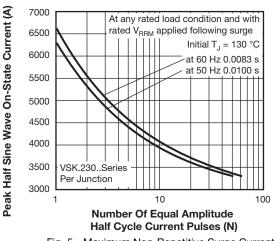


Fig. 4 - On-State Power Loss Characteristics

### VS-VSK.230..PbF Series

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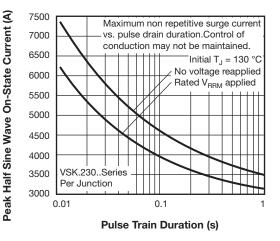


Fig. 6 - Maximum Non-Repetitive Surge Current

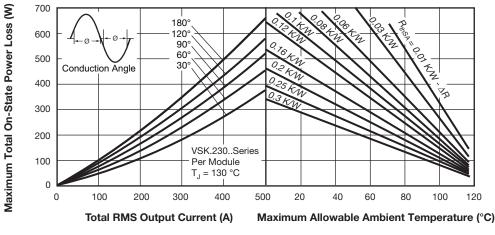


Fig. 7 - On-State Power Loss Characteristics

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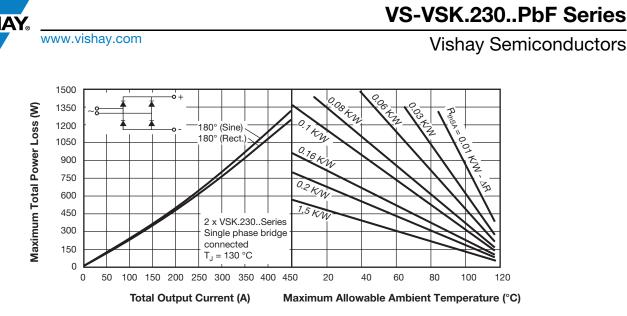


Fig. 8 - On-State Power Loss Characteristics

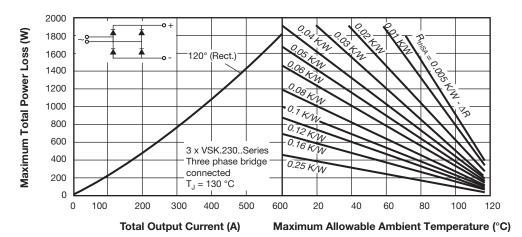
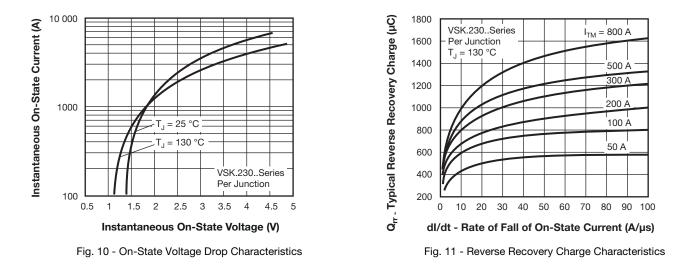


Fig. 9 - On-State Power Loss Characteristics



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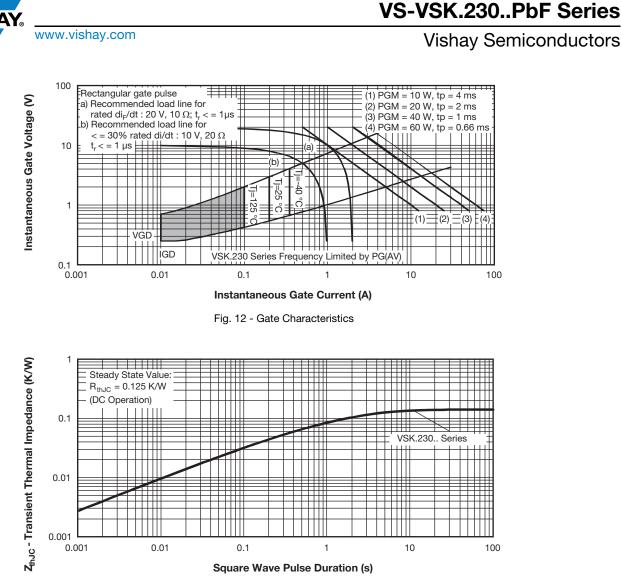


Fig. 13 - Thermal Impedance Z<sub>thJC</sub> Characteristics

#### **ORDERING INFORMATION TABLE**

Device code	vs-v	vs	кт	230	-	20	PbF		
		)	2	3		4	5		
	1	-	Vishay	Semicor	nductors	product			
	2	-	Circuit	configura	ation (see	e dimensi	ons - link	at the end of datasheet)	
	3	-	Curren	Current rating					
	4	-	Voltage	e code x	100 = V <sub>R</sub>	RRM (see	Voltage F	Ratings table)	
	5	-	<ul> <li>None = standard production</li> <li>PbF = lead (Pb)-free</li> </ul>						

#### Note

To order the optional hardware go to <u>www.vishay.com/doc?95172</u>

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CIRCUIT CONFIGURATION									
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING							
Two SCRs doubler circuit	КТ	VSKT							
SCR/diode doubler circuit, positive control	КН	VSKH							
SCR/diode doubler circuit, negative control	KL	VSKL							
Two SCRs common cathodes	КК	VSKK							

LINKS TO RELATED DOCUMENTS				
Dimensions	www.vishay.com/doc?95086			

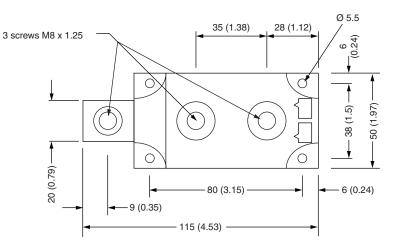


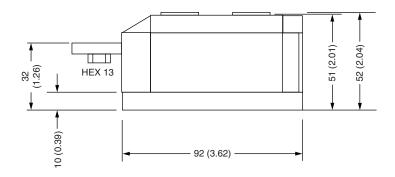
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# MAGN-A-PAK

#### **DIMENSIONS** in millimeters (inches)





#### Notes

- Dimensions are nominal
- Full engineering drawings are available on request
- UL identification number for gate and cathode wire: UL 1385
- UL identification number for package: UL 94 V-0



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