Inverter Grade Thyristors (Hockey PUK Version), 620 A

B-PUK (TO-200AC)

FEATURES

- Metal case with ceramic insulator
- All diffused design
- Center amplifying gate
- Guaranteed high dV/dt
- Guaranteed high dI/dt
- International standard case B-PUK (TO-200AC)
- High surge current capability
- Low thermal impedance
- High speed performance
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free RoHS COMPLIANT

TYPICAL APPLICATIONS

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

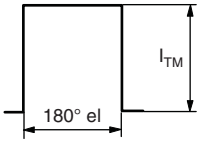
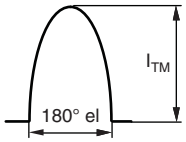
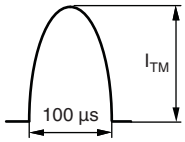
PRIMARY CHARACTERISTICS	
Package	B-PUK (TO-200AC)
Circuit configuration	Single SCR
$I_{T(AV)}$	620 A
V_{DRM}/V_{RRM}	400 V, 800 V
V_{TM}	1.96 V
I_{TSM} at 50 Hz	11 000 A
I_{TSM} at 60 Hz	11 500 A
I_{GT}	200 mA
T_C/T_{hs}	55 °C

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		620	A
	T_{hs}	55	°C
$I_{T(RMS)}$		1230	A
	T_{hs}	25	°C
I_{TSM}	50 Hz	11 000	A
	60 Hz	11 500	
I^2t	50 Hz	605	kA^2s
	60 Hz	553	
V_{DRM}/V_{RRM}		400 to 800	V
t_q	Range	10 to 30	µs
T_J		-40 to +125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM}, MAXIMUM REPETITIVE PEAK VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST333C..L	04	400	500	50
	08	800	900	

CURRENT CARRYING CAPABILITY

FREQUENCY							UNITS
50 Hz	1430	1250	2340	1940	6310	5620	A
400 Hz	1670	1170	2310	1940	3440	5030	A
1000 Hz	1080	880	2090	1800	2040	1750	A
2500 Hz	530	400	1190	990	990	800	A
Recovery voltage V_R	50		50		50		V
Voltage before turn-on V_D	V_{DRM}		V_{DRM}		V_{DRM}		V
Rise of on-state current dI/dt	50		-		-		A/µs
Heatsink temperature	40	55	40	55	40	55	°C
Equivalent values for RC circuit	10 / 0.47		10 / 0.47		10 / 0.47		Ω/µF

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled			620 (305)	A
					55 (75)	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 °C heatsink temperature double side cooled			1230	A
Maximum peak, one half cycle, non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ max.	11 000	A
		t = 8.3 ms			11 500	A
		t = 10 ms	100 % V_{RRM} reapplied		9250	A
		t = 8.3 ms			9700	A
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		605	kA^2s
		t = 8.3 ms			553	kA^2s
		t = 10 ms	100 % V_{RRM} reapplied		428	kA^2s
		t = 8.3 ms			391	kA^2s
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied			6050	$kA^2\sqrt{s}$
Maximum peak on-state voltage	V_{TM}	I_{TM} = 1810 A, $T_J = T_J$ maximum, t_p = 10 ms sine wave pulse			1.96	V
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ max.			0.91	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.93	V
Low level value of forward slope resistance	r_{t1}	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ max.			0.58	mΩ
High level value of forward slope resistance	r_{t2}	(I > π x $I_{T(AV)}$), $T_J = T_J$ max.			0.58	mΩ
Maximum holding current	I_H	T_J = 25 °C, I_T > 30 A			600	mA
Typical latching current	I_L	T_J = 25 °C, V_A = 12 V, R_a = 6 Ω, I_G = 1 A			1000	mA

SWITCHING

PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current		dI/dt	$T_J = T_J$ max., V_{DRM} = rated V_{DRM}, I_{TM} = 2 x dI/dt	1000	A/µs
Typical delay time		t_d	T_J = 25 °C, V_{DM} = rated V_{DRM}, I_{TM} = 50 A DC, t_p = 1 µs Resistive load, gate pulse: 10 V, 5 Ω source	1.1	µs
Maximum turn-off time	minimum	t_q	$T_J = T_J$ max., I_{TM} = 550 A, commutating dI/dt = 40 A/µs, V_R = 50 V, t_p = 500 µs, dV/dt: see table in device code	10	µs
	maximum			30	µs

BLOCKING				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ max., linear to 80 % V_{DRM}, higher value available on request	500	V/µs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	$T_J = T_J$ max., rated V_{DRM}/V_{RRM} applied	50	mA

TRIGGERING				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Maximum peak gate power	P_{GM}	$T_J = T_J$ max., f = 50 Hz, d % = 50	60	W
Maximum average gate power	$P_{G(AV)}$		10	
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ max., $t_p \leq 5$ ms	10	A
Maximum peak positive gate voltage	$+V_{GM}$		20	V
Maximum peak negative gate voltage	$-V_{GM}$		5	
Maximum DC gate current required to trigger	I_{GT}	T_J = 25 °C, V_A = 12 V, R_a = 6 Ω	200	mA
Maximum DC gate voltage required to trigger	V_{GT}		3	V
Maximum DC gate current not to trigger	I_{GD}	$T_J = T_J$ max., rated V_{DRM} applied	20	mA
Maximum DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Maximum operating junction temperature range	T_J		-40 to +125	°C
Maximum storage temperature range	T_{Stg}		-40 to +150	
Maximum thermal resistance, junction to heatsink	$R_{thJ\text{-}hs}$	DC operation single side cooled	0.11	K/W
		DC operation double side cooled	0.05	
Maximum thermal resistance, case to heatsink	$R_{thC\text{-}hs}$	DC operation single side cooled	0.011	
		DC operation double side cooled	0.005	
Mounting force, ± 10 %			9800 (1000)	N (kg)
Approximate weight			250	g
Case style		See dimensions - link at the end of datasheet	TO-200AC (B-PUK)	

$\Delta R_{thJ\text{-}hs}$ CONDUCTION						
CONDUCTION ANGLE	**SINUSOIDAL CONDUCTION**		**RECTANGULAR CONDUCTION**		**TEST CONDITIONS**	**UNITS**
	SINGLE SIDE	**DOUBLE SIDE**	**SINGLE SIDE**	**DOUBLE SIDE**		
180°	0.012	0.010	0.008	0.008	$T_J = T_J$ max.	K/W
120°	0.014	0.015	0.014	0.014		
90°	0.018	0.018	0.019	0.019		
60°	0.026	0.027	0.027	0.028		
30°	0.045	0.046	0.046	0.046		

Note

- The table above shows the increment of thermal resistance $R_{thJ\text{-}hs}$ when devices operate at different conduction angles than DC

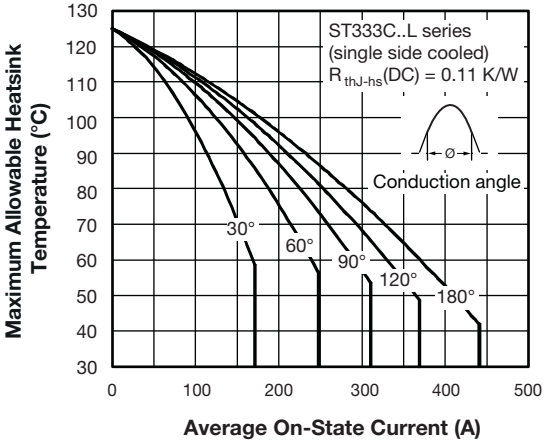


Fig. 1 - Current Ratings Characteristics

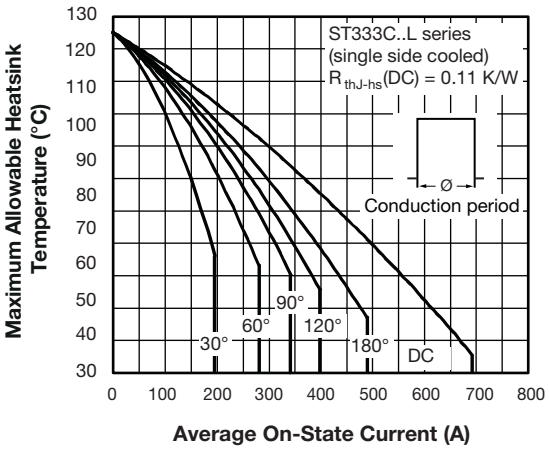


Fig. 2 - Current Ratings Characteristics

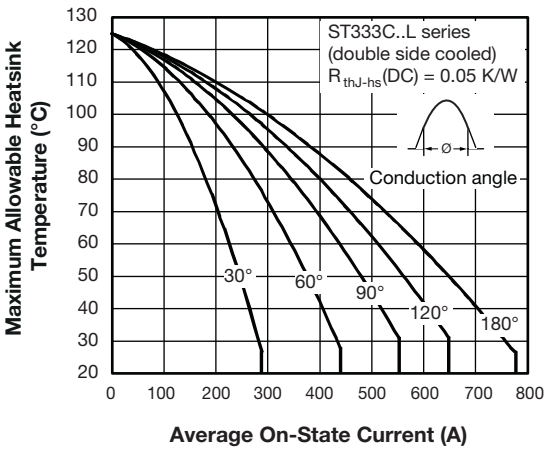


Fig. 3 - Current Ratings Characteristics

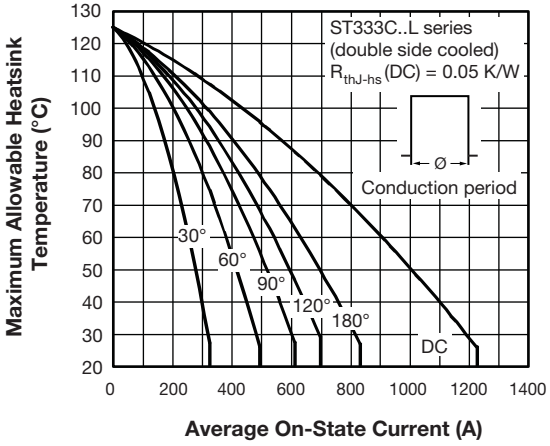


Fig. 4 - Current Ratings Characteristics

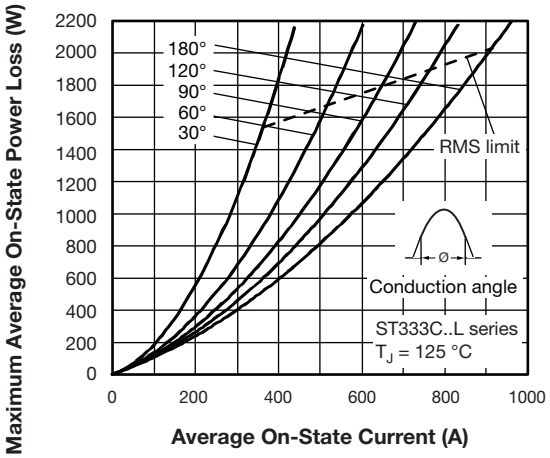


Fig. 5 - On-State Power Loss Characteristics

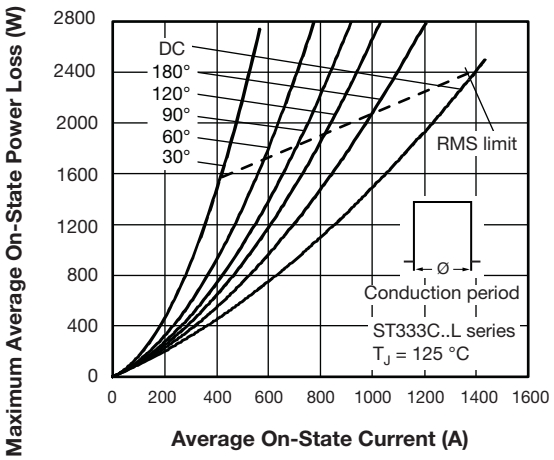


Fig. 6 - On-State Power Loss Characteristics

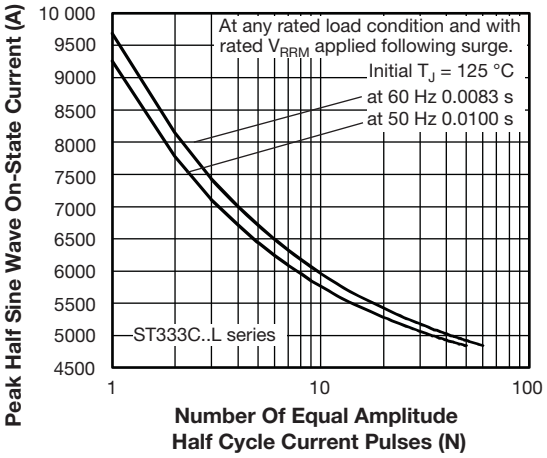


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

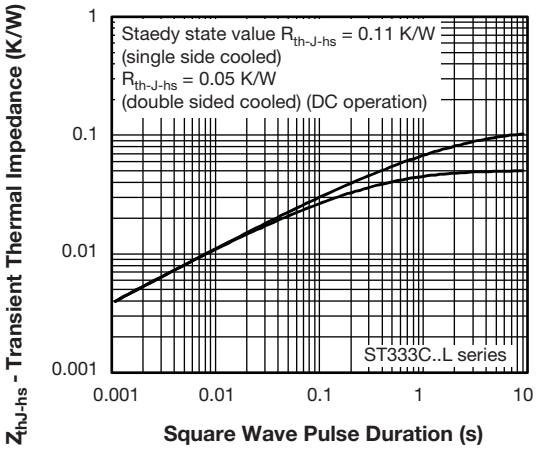


Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics

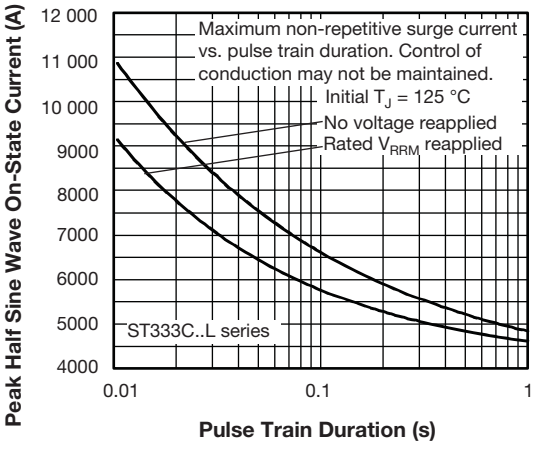


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

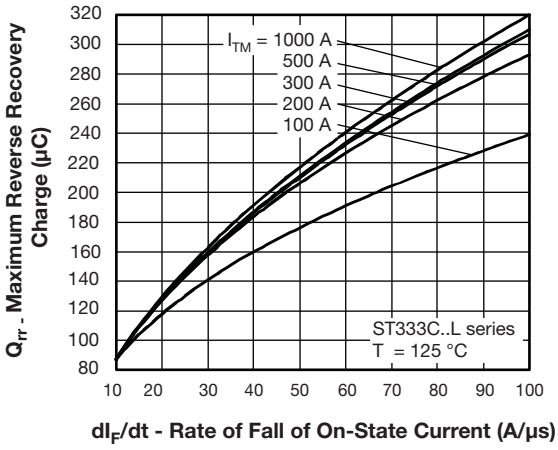


Fig. 11 - Reverse Recovered Charge Characteristics

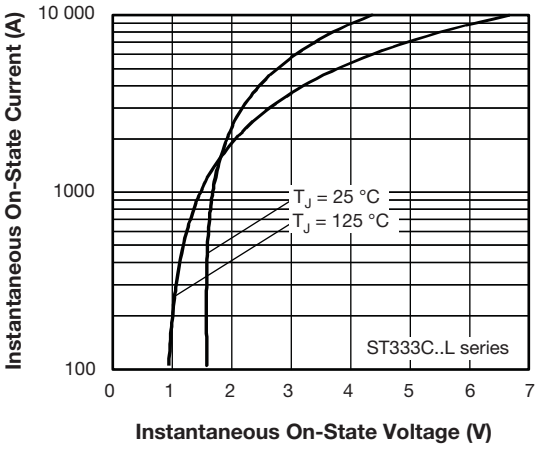


Fig. 9 - On-State Voltage Drop Characteristics

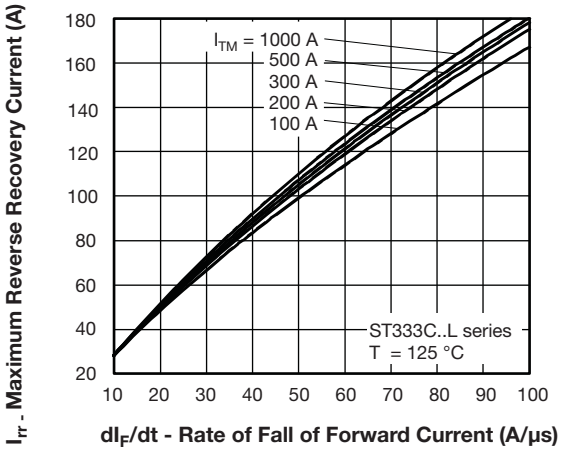


Fig. 12 - Reverse Recovery Current Characteristics

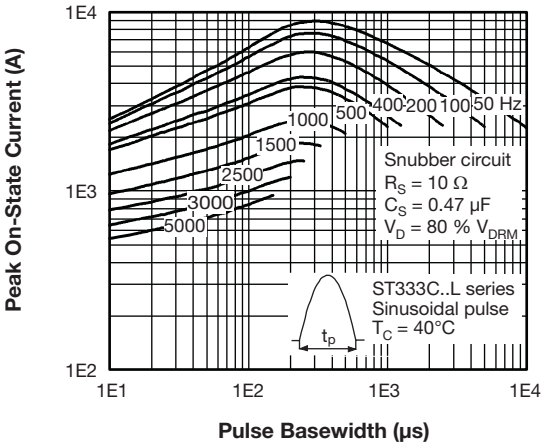


Fig. 13a - Frequency Characteristics

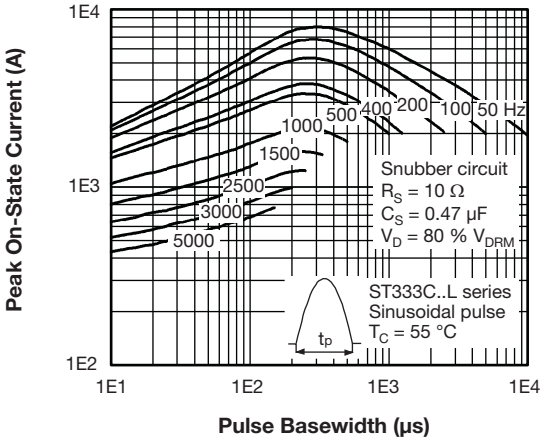


Fig.13b - Frequency Characteristics

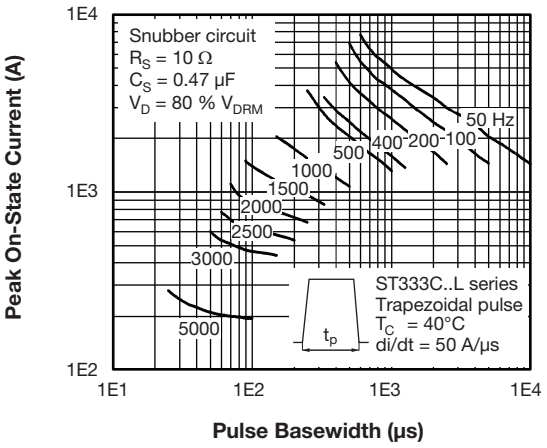


Fig.14a - Frequency Characteristics

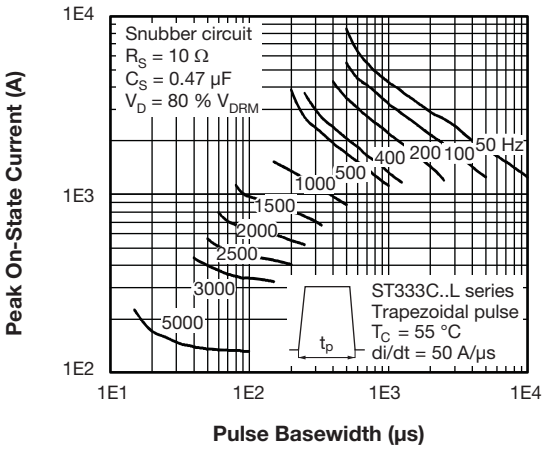


Fig.14b - Frequency Characteristics

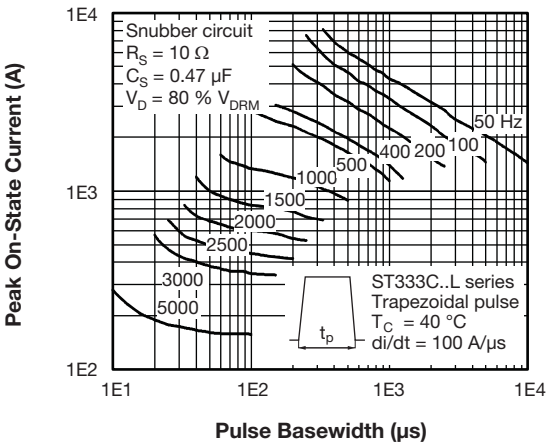


Fig.15a - Maximum On-State Energy Power Loss Characteristics

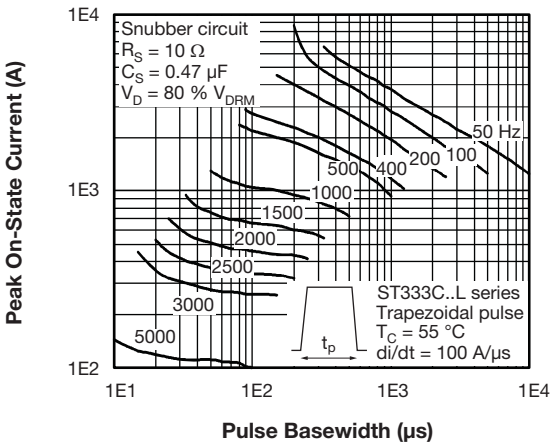


Fig.15b - Maximum On-State Energy Power Loss Characteristics

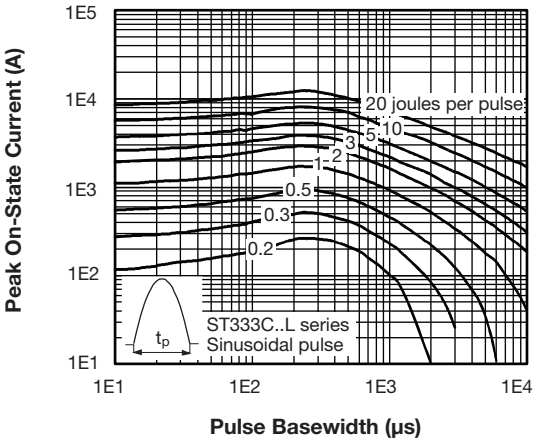


Fig.16a - Maximum On-State Energy Power Loss Characteristics

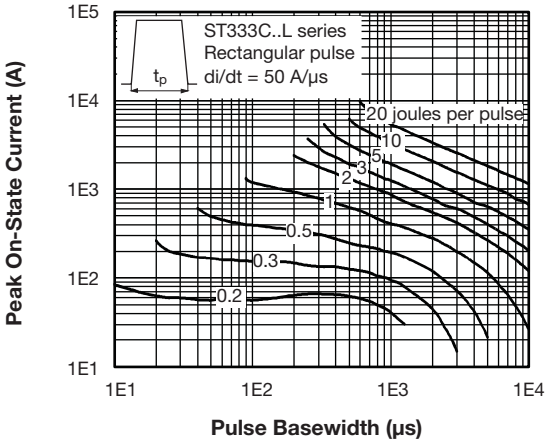


Fig.16b - Maximum On-State Energy Power Loss Characteristics

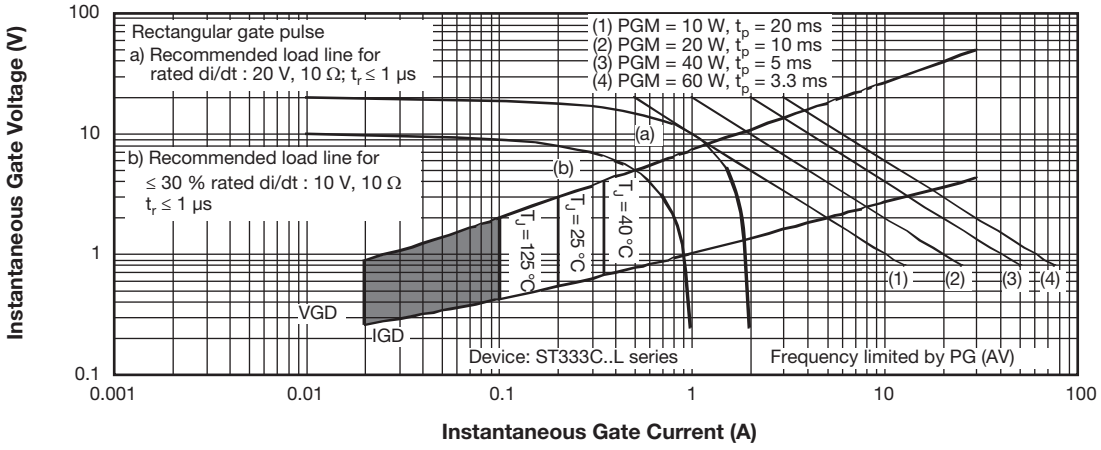


Fig.17 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code

VS-	ST	33	3	C	08	L	H	K	1	-
1	2	3	4	5	6	7	8	9	10	11

1 - Vishay Semiconductors product

2 - Thyristor

3 - Essential part number

4 - 3 = fast turn-off

5 - C = ceramic PUK

6 - Voltage code x 100 = V_{RRM}
(see Voltage Ratings table)

7 - L = PUK case B-PUK (TO-200AC)

8 - Reapplied dV/dt code (for t_q test condition)

9 - t_q code

10 - 0 = eyelet terminals
(gate and auxiliary cathode unsoldered leads)
1 = fast-on terminals
(gate and auxiliary cathode unsoldered leads)
2 = eyelet terminals
(gate and auxiliary cathode soldered leads)
3 = fast-on terminals
(gate and auxiliary cathode soldered leads)

11 - Critical dV/dt:
- None = 500 V/µs (standard value)
- L = 1000 V/µs (special selection)

dV/dt - t_q combinations available

	dV/dt (V/µs)	20	50	100	200	400
t_q (µs)	10	CN	DN	EN	-	-
	12	CM	DM	EM	**FM***	-
	15	CL	DL	EL	**FL***	HL
	18	CP	DP	EP	FP	HP
	20	CK	DK	EK	FK	H
	25	--	--	--	FJ	HJ
	30	--	--	--	--	HH

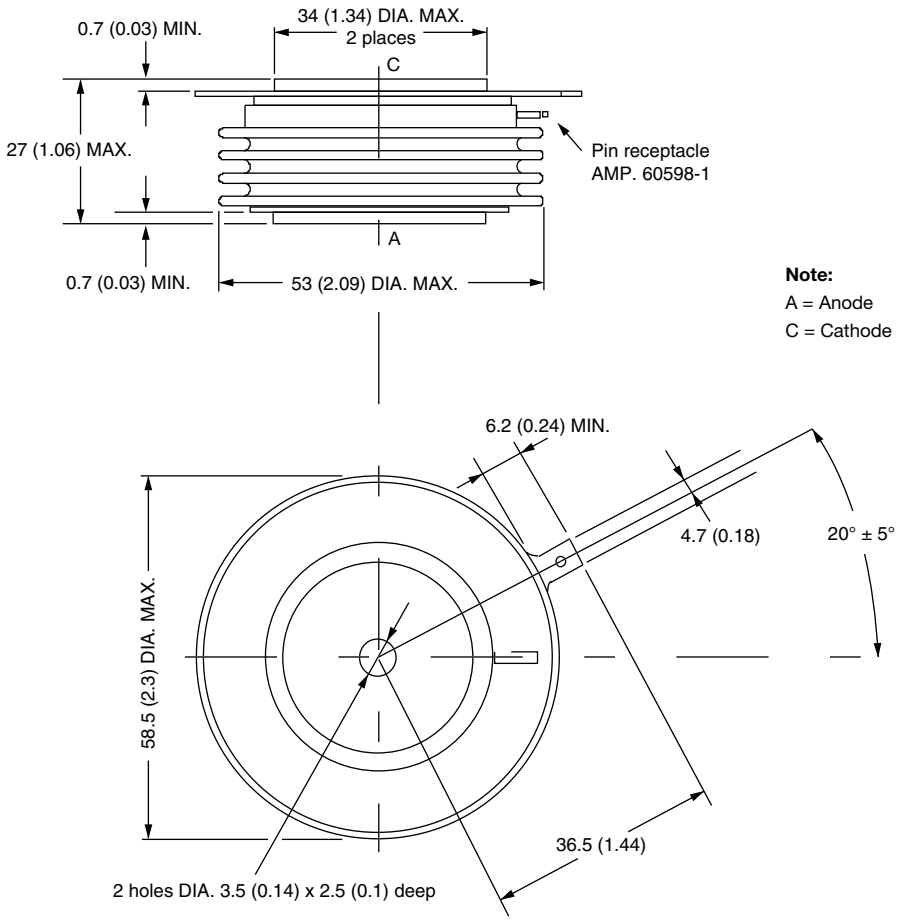
* Standard part number.
All other types available only on request.

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95076

B-PUK (TO-200AC)

DIMENSIONS in millimeters (inches)

Creepage distance: 36.33 (1.430) minimum
Strike distance: 17.43 (0.686) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)

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