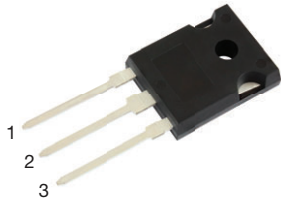
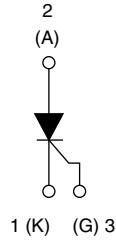


## Thyristor High Voltage, Phase Control SCR, 50 A



TO-247AD 3L



### FEATURES

- AEC-Q101 qualified, meets JESD 201 class 1A whisker test
- Flexible solution for reliable AC power rectification
- Easy control peak current at charger power up to reduce passive / electromechanical components
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- On-board and off-board EV / HEV battery chargers
- Renewable energy inverters

### DESCRIPTION

The VS-50TPS12 high voltage series of silicon controlled rectifiers are specifically designed for medium power switching, and phase control applications.

PRIMARY CHARACTERISTICS	
$I_{T(AV)}$	50 A
$V_{DRM}/V_{RRM}$	1200 V
$V_{TM}$ (typ.)	1.2 V
$I_{GT}$ (typ.)	45 mA
$T_J$ max.	150 °C
Package	TO-247AD 3L
Circuit configuration	Single SCR

MAJOR RATINGS AND CHARACTERISTICS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage	$V_{RRM} / V_{DRM}$		1200	V
On-state voltage	$V_T$	50 A, $T_J = 125\text{ °C}$	1.2	
Average rectified forward current	$I_{T(AV)}$		50	A
Maximum continuous RMS on-state current	$I_{RMS}$		79	
Non-repetitive peak surge current	$I_{TSM}$		630	
Maximum rate of rise	$dv/dt$		1000	V/ $\mu$ s
Operating junction and storage temperature range	$T_J, T_{Stg}$		-40 to +150	°C

VOLTAGE RATINGS			
PART NUMBER	$V_{RRM} / V_{DRM}$ , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$I_{RRM} / I_{DRM}$ AT 150 °C mA
VS-50TPS12LHM3	1200	1300	70



ABSOLUTE MAXIMUM RATINGS						
PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Maximum average on-state current	$I_{T(AV)}$	$T_C = 112\text{ }^\circ\text{C}$ , 180° conduction half sine wave		-	50	A
Maximum continuous RMS on-state current as AC switch	$I_{T(RMS)}$			-	79	
Peak, one-cycle non-repetitive surge current	$I_{TSM}$	10 ms sine pulse, rated $V_{RRM}$ applied	Initial $T_J = T_J$ maximum	-	530	
		10 ms sine pulse, no voltage reapplied		-	630	
$I^2t$ for fusing	$I^2t$	10 ms sine pulse, rated $V_{RRM}$ applied		-	1405	A <sup>2</sup> s
		10 ms sine pulse, no voltage reapplied	-	1986		
$I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	$t = 0.1\text{ ms to }10\text{ ms}$ , no voltage reapplied, $T_J = 125\text{ }^\circ\text{C}$		-	19 850	A <sup>2</sup> √s
Low level value of threshold voltage	$V_{T(TO)1}$	$T_J = 125\text{ }^\circ\text{C}$		-	0.89	V
High level value of threshold voltage	$V_{T(TO)2}$			-	0.97	
Low level value of on-state slope resistance	$r_{t1}$			-	6.77	mΩ
High level value of on-state slope resistance	$r_{t2}$			-	6.32	
On-state voltage	$V_T$	50 A, $T_J = 25\text{ }^\circ\text{C}$		1.2	1.32	V
		100 A, $T_J = 25\text{ }^\circ\text{C}$		1.4	1.6	
Rate of rise of turned-on current	$di/dt$	$T_J = 25\text{ }^\circ\text{C}$		-	150	A/μs
Holding current	$I_H$	Anode supply = 6 V, resistive load, $T_J = 25\text{ }^\circ\text{C}$		-	300	mA
Latching current	$I_L$			-	350	
Reverse and direct leakage current	$I_{RRM}/I_{DRM}$	$T_J = 25\text{ }^\circ\text{C}$		-	0.05	mA
		$T_J = 150\text{ }^\circ\text{C}$		-	70	
Rate of rise of off-state voltage	$dv/dt$	$T_J = T_J$ maximum, linear to 80 % $V_{DRM}$ , $R_g\text{-k} = 100\text{ }^\circ\Omega$		-	1000	V/μs

TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Peak gate power	$P_{GM}$	10 ms sine pulse, no voltage reapplied		-	10	W
Average gate power	$P_{G(AV)}$			-	2.5	
Peak gate current	$I_{GM}$			-	2.5	A
Peak negative gate voltage	$-V_{GM}$			-	10	V
Required DC gate voltage to trigger	$V_{GT}$	$T_J = -40\text{ }^\circ\text{C}$	Anode supply = 6 V resistive load	-	1.6	
		$T_J = 25\text{ }^\circ\text{C}$		-	1.5	
		$T_J = 150\text{ }^\circ\text{C}$		-	1	
Required DC gate to trigger	$I_{GT}$	$T_J = -40\text{ }^\circ\text{C}$	Anode supply = 6 V resistive load	-	160	mA
		$T_J = 25\text{ }^\circ\text{C}$		45	100	
		$T_J = 150\text{ }^\circ\text{C}$		-	60	
DC gate voltage not to trigger	$V_{GD}$	$T_J = 150\text{ }^\circ\text{C}$ , $V_{DRM} = \text{rated value}$		-	0.2	V
DC gate current not to trigger	$I_{GD}$			-	3	mA

SWITCHING						
PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Turn-on time	$t_{gt}$	$I_T = 50\text{ A}$ , $V_D = 50\% V_{DRM}$ , $I_{gt} = 300\text{ mA}$ , $T_J = 25\text{ }^\circ\text{C}$		1.5	-	μs
Turn-off time	$t_q$	$I_T = 50\text{ A}$ , $V_D = 80\% V_{DRM}$ , $dV/dt = 20\text{ V}/\mu\text{s}$ , $t_p = 200\text{ }^\mu\text{s}$ , $I_{gt} = 100\text{ mA}$ , $dI/dt = 10\text{ A}/\mu\text{s}$ , $V_R = 100\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$		92	-	



THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS	TYP.	MAX.	UNITS
Maximum junction and storage temperature range	$T_J, T_{Stg}$		-40	150	°C
Maximum thermal resistance, junction to case	$R_{thJC}$		-	0.35	°C/W
Maximum thermal resistance, junction to ambient	$R_{thJA}$		-	40	
Typical thermal resistance, case to heatsink	$R_{thCS}$	Mounting surface, smooth, and greased	0.2	-	
Mounting torque	minimum		6 (5)		kgf · cm (lbf · in)
	maximum		12 (10)		
Marking device		Case style Super TO-247AD 3L	50TPS12LH		

$\Delta R_{thJ-HS}$ CONDUCTION PER JUNCTION											
DEVICE	SINE HALF-WAVE CONDUCTION					RECTANGULAR WAVE CONDUCTION					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VS-50TPS12LHM3	0.143	0.166	0.208	0.299	0.490	0.099	0.168	0.223	0.311	0.494	°C/W

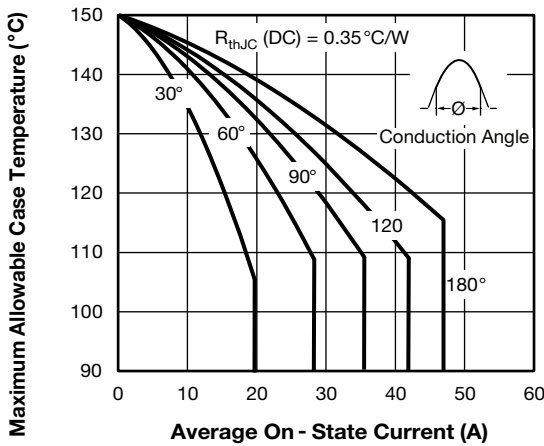


Fig. 1 - Current Rating Characteristics

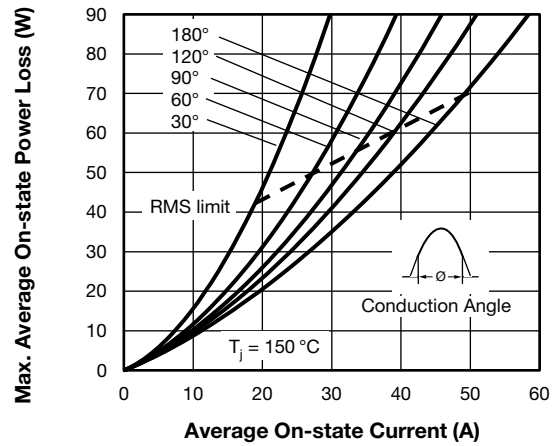


Fig. 3 - On-State Power Loss Characteristics

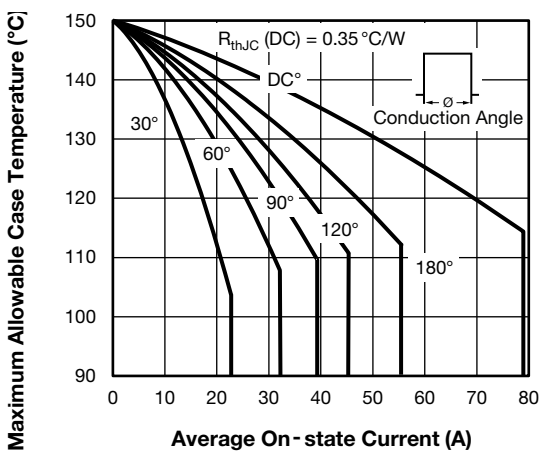


Fig. 2 - Current Rating Characteristics

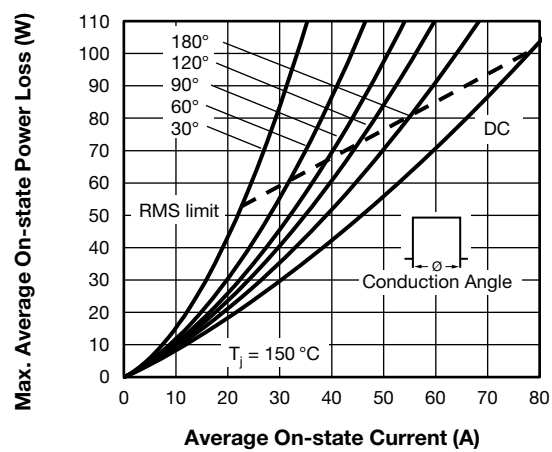


Fig. 4 - On-State Power Loss Characteristics

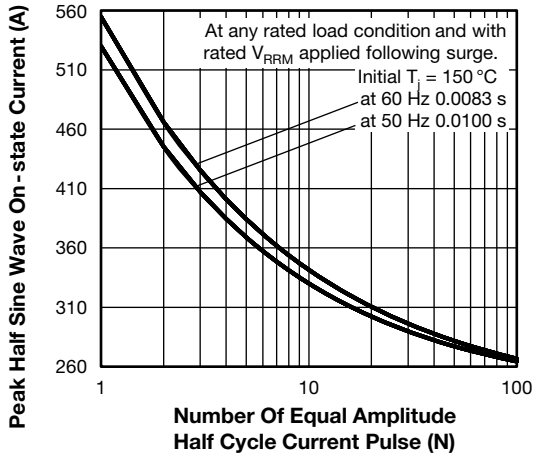


Fig. 5 - Maximum Non-Repetitive Surge Current

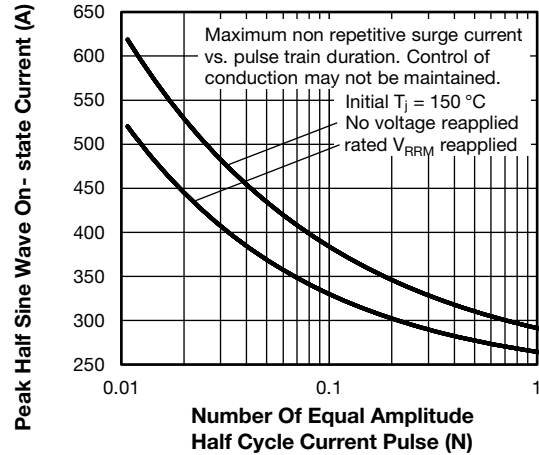


Fig. 6 - Maximum Non-Repetitive Surge Current

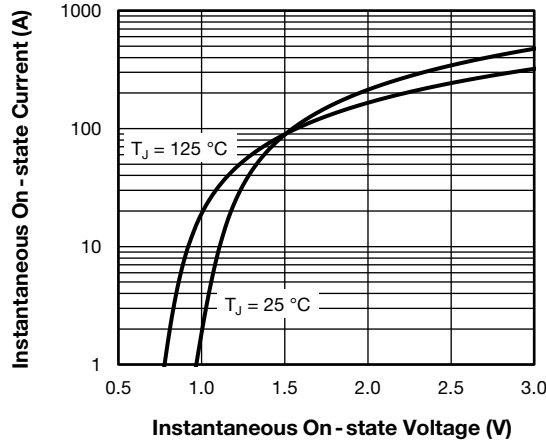


Fig. 7 - On-State Voltage Drop Characteristics

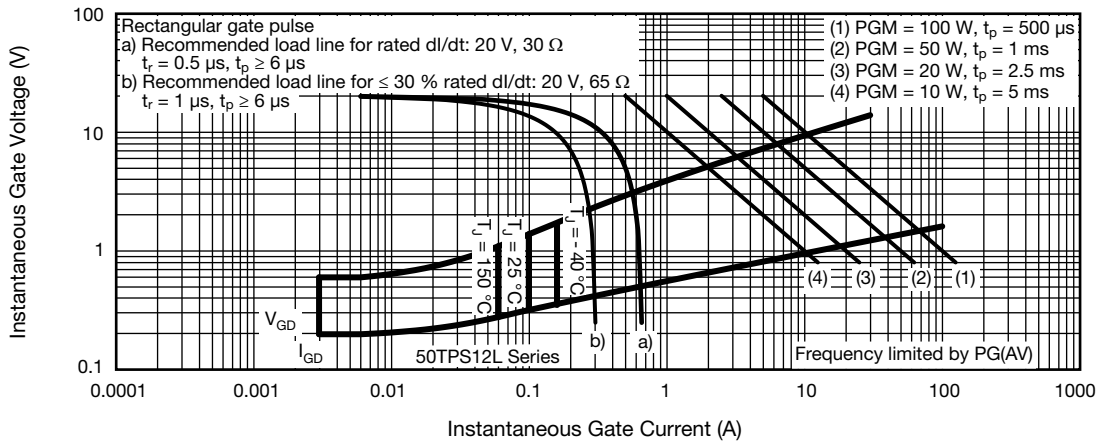


Fig. 8 - Gate Characteristics

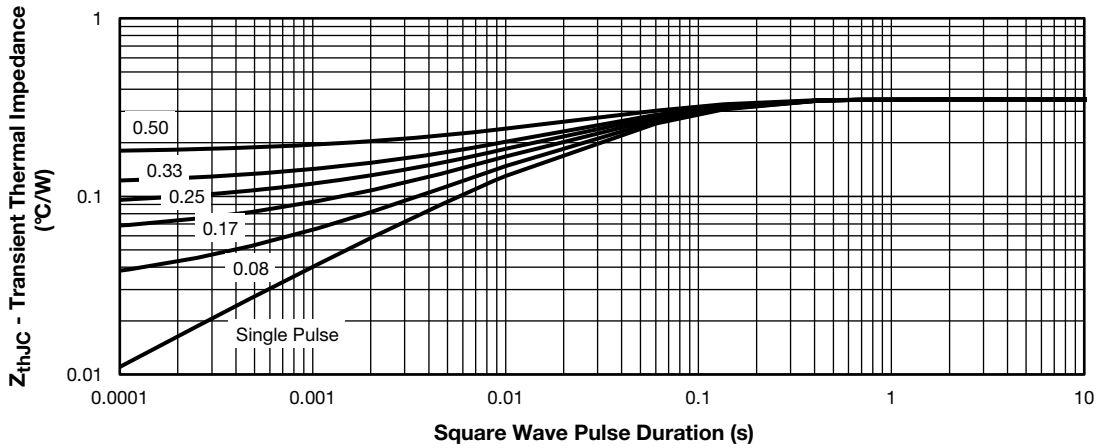


Fig. 9 - Thermal Impedance  $Z_{thJC}$  Characteristics

**ORDERING INFORMATION TABLE**

Device code	<b>VS-</b>	<b>50</b>	<b>T</b>	<b>P</b>	<b>S</b>	<b>12</b>	<b>L</b>	<b>H</b>	<b>M3</b>
	①	②	③	④	⑤	⑥	⑦	⑧	⑨

- 1** - Vishay Semiconductors product
- 2** - Current code (50 = 50 A)
- 3** - Circuit configuration:  
T = thyristor
- 4** - P = TO-247AD package
- 5** - Type of silicon:  
S = standard recovery rectifier
- 6** - Voltage code (12 = 1200 V)
- 7** - Package L = long lead
- 8** - H = AEC-Q101 qualified
- 9** - M3 = halogen-free, RoHS-compliant, and terminations lead (Pb)-free

<b>ORDERING INFORMATION</b> (example)			
PREFERRED P/N	QUANTITY PER TUBE	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION
VS-50TPS12LHM3	25	contact factory	Antistatic plastic tubes

<b>LINKS TO RELATED DOCUMENTS</b>		
Dimensions	TO-247AD 3L	<a href="http://www.vishay.com/doc?95626">www.vishay.com/doc?95626</a>
Part marking information	TO-247AD 3L	<a href="http://www.vishay.com/doc?95007">www.vishay.com/doc?95007</a>

### TO-247AD 3L

**DIMENSIONS** in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES	SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.			MIN.	MAX.	MIN.	MAX.	
A	4.65	5.31	0.183	0.209		D2	0.51	1.30	0.020	0.051	
A1	2.21	2.59	0.087	0.102		E	15.29	15.87	0.602	0.625	3
A2	1.50	2.49	0.059	0.098		E1	13.46	-	0.53	-	
b	0.99	1.40	0.039	0.055		e	5.46 BSC		0.215 BSC		
b1	0.99	1.35	0.039	0.053		Ø K	0.254		0.010		
b2	1.65	2.39	0.065	0.094		L	19.81	20.32	0.780	0.800	
b3	1.65	2.34	0.065	0.092		L1	3.71	4.29	0.146	0.169	
b4	2.59	3.43	0.102	0.135		Ø P	3.56	3.66	0.14	0.144	
b5	2.59	3.38	0.102	0.133		Ø P1	-	6.98	-	0.275	
c	0.38	0.89	0.015	0.035		Q	5.31	5.69	0.209	0.224	
c1	0.38	0.84	0.015	0.033		R	4.52	5.49	0.178	0.216	
D	19.71	20.70	0.776	0.815	3	S	5.51 BSC		0.217 BSC		
D1	13.08	-	0.515	-	4						

**Notes**

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC® outline TO-247 with exception of dimension A min., D, E min., Q min., S, and note 4



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