



Phase Control Thyristors (Stud Version), 230 A



TO-93 (TO-209AB)

FEATURES

- Center amplifying gate
- International standard case TO-93 (TO-209AB)
- Glass-metal seal up to 1200 V
- Compression bonded encapsulation for heavy duty operations such as severe thermal cycling
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS
COMPLIANT

PRIMARY CHARACTERISTICS

$I_{T(AV)}$	230 A
V_{DRM}/V_{RRM}	400 V, 800 V, 1200 V
V_{TM}	1.55 V
I_{GT}	150 mA
T_J	-40 °C to +125 °C
Package	TO-93 (TO-209AB)
Circuit configuration	Single SCR

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		230	A
	T_C	85	°C
$I_{T(RMS)}$		360	A
I_{TSM}	50 Hz	5700	A
	60 Hz	5970	
I^2t	50 Hz	163	kA ² s
	60 Hz	149	
V_{DRM}/V_{RRM}		400 to 1200	V
t_q	Typical	100	μs
T_J		-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST230S	04	400	500	30
	08	800	900	
	12	1200	1300	

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave	230	A
			85	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 78 °C case temperature	360	
Maximum peak, one-cycle non-repetitive surge current	I_{TSM}	<div> <div> $t = 10 \text{ ms}$ $t = 8.3 \text{ ms}$ </div> <div> No voltage reappplied 100 % V_{RRM} reappplied </div> </div>	5700 5970 4800 5000	A
		Sinusoidal half wave, initial $T_J = T_J$ maximum		
Maximum I^2t for fusing	I^2t	<div> $t = 10 \text{ ms}$ $t = 8.3 \text{ ms}$ </div> <div> No voltage reappplied 100 % V_{RRM} reappplied </div>	163 148 115 105	kA^2s
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	$t = 0.1$ to 10 ms , no voltage reappplied	1630	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7 \% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ maximum	0.92	V
High level value of threshold voltage	$V_{T(TO)2}$	$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ maximum	0.98	
Low level value of on-state slope resistance	r_{t1}	$(16.7 \% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ maximum	0.88	$m\Omega$
High level value of on-state slope resistance	r_{t2}	$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ maximum	0.81	
Maximum on-state voltage	V_{TM}	$I_{pk} = 720 \text{ A}$, $T_J = T_J$ maximum, $t_p = 10 \text{ ms}$ sine pulse	1.55	V
Maximum holding current	I_H	$T_J = 25 \text{ }^\circ\text{C}$, anode supply 12 V resistive load	600	mA
Maximum (typical) latching current	I_L		1000 (300)	

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	Gate drive 20 V, 20 Ω , $t_r \leq 1 \mu s$ $T_J = T_J$ maximum, anode voltage $\leq 80 \% V_{DRM}$	1000	A/ μs
Typical delay time	t_d	Gate current 1 A, $di_g/dt = 1 \text{ A}/\mu s$ $V_d = 0.67 \% V_{DRM}$, $T_J = 25 \text{ }^\circ\text{C}$	1.0	μs
Typical turn-off time	t_q	$I_{TM} = 300 \text{ A}$, $T_J = T_J$ maximum, $di_f/dt = 20 \text{ A}/\mu s$, $V_R = 50 \text{ V}$, $dV/dt = 20 \text{ V}/\mu s$, gate 0 V 100 Ω , $t_p = 500 \mu s$	100	

BLOCKING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}	500	V/ μs
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	30	mA



TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES		UNITS
				TYP.	MAX.	
Maximum peak gate power	P _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		10.0		W
Maximum average gate power	P _{G(AV)}	T _J = T _J maximum, f = 50 Hz, d% = 50		2.0		
Maximum peak positive gate current	I _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		3.0		A
Maximum peak positive gate voltage	+V _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		20		V
Maximum peak negative gate voltage	-V _{GM}			5.0		
DC gate current required to trigger	I _{GT}	T _J = - 40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	180	-	
		T _J = 25 °C		90	150	mA
		T _J = 125 °C		40	-	
DC gate voltage required to trigger	V _{GT}	T _J = - 40 °C		2.9	-	V
		T _J = 25 °C		1.8	3.0	
		T _J = 125 °C		1.2	-	
DC gate current not to trigger	I _{GD}	T _J = T _J maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V _{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V _{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum operating junction temperature range	T_J			-40 to 125	°C
Maximum storage temperature range	T_{Stg}			-40 to 150	
Maximum thermal resistance, junction to case	R_{thJC}	DC operation		0.10	K/W
Maximum thermal resistance, case to heatsink	R_{thC-hs}	Mounting surface, smooth, flat and greased		0.04	
Mounting torque, ± 10 %		Non-lubricated threads		31 (275)	N · m (lbf · in)
		Lubricated threads		24.5 (210)	
Approximate weight				280	g
Case style		See dimensions - link at the end of datasheet		TO-93 (TO-209AB)	

ΔR_{thJC} CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.016	0.012	$T_J = T_J$ maximum	K/W
120°	0.019	0.020		
90°	0.025	0.027		
60°	0.036	0.037		
30°	0.060	0.060		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

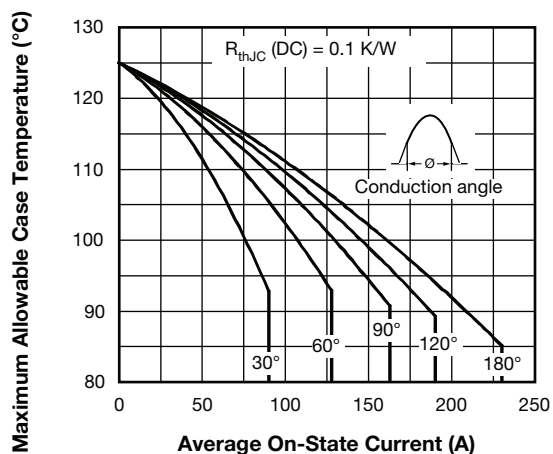


Fig. 1 - Current Ratings Characteristics

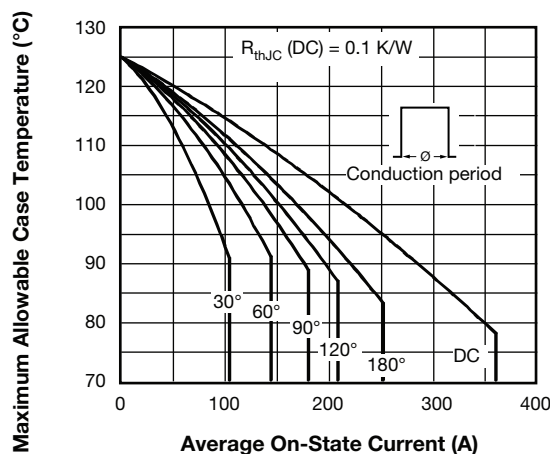


Fig. 2 - Current Ratings Characteristics

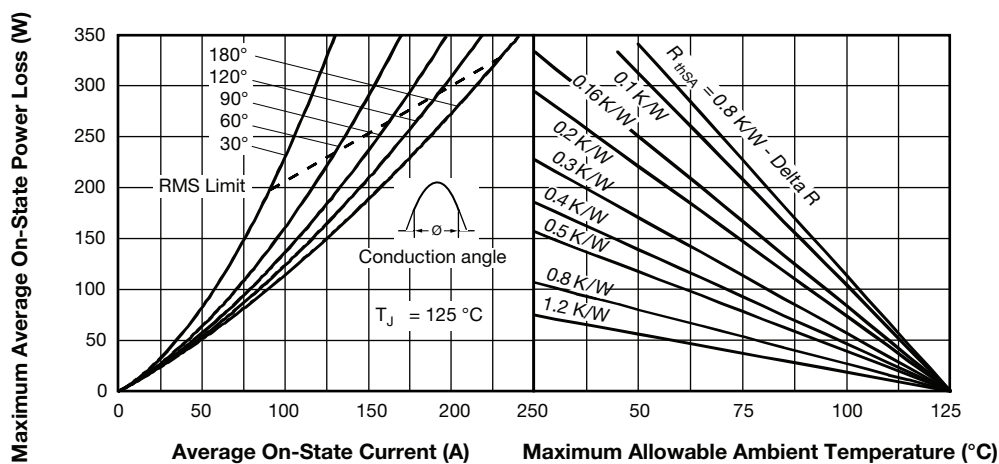


Fig. 3 - On-State Power Loss Characteristics

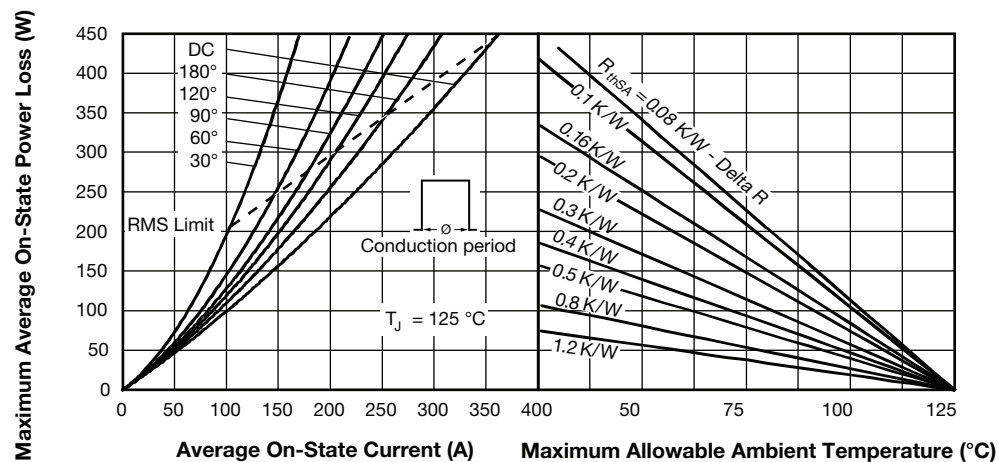


Fig. 4 - On-State Power Loss Characteristics

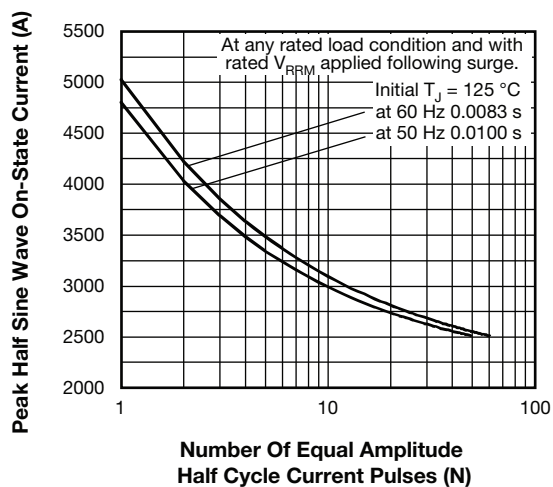


Fig. 5 - Maximum Non-Repetitive Surge Current

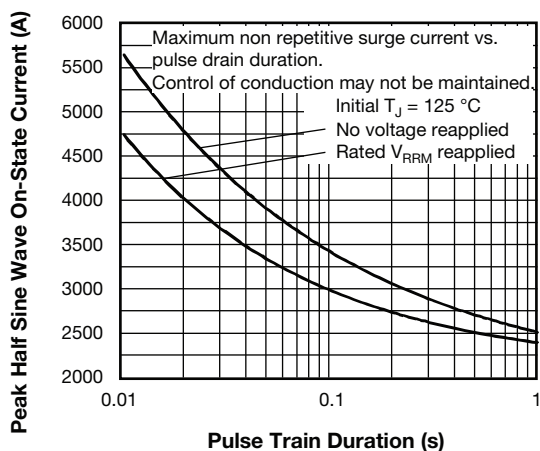


Fig. 6 - Maximum Non-Repetitive Surge Current

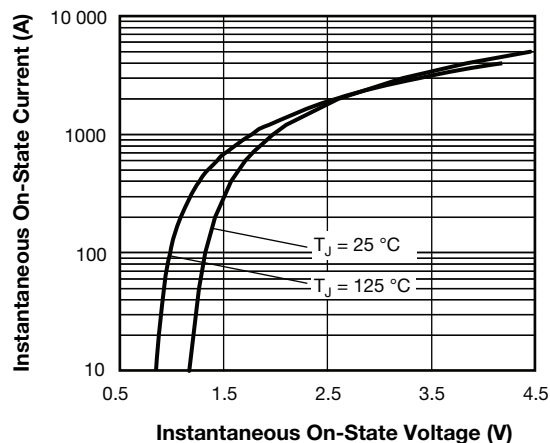
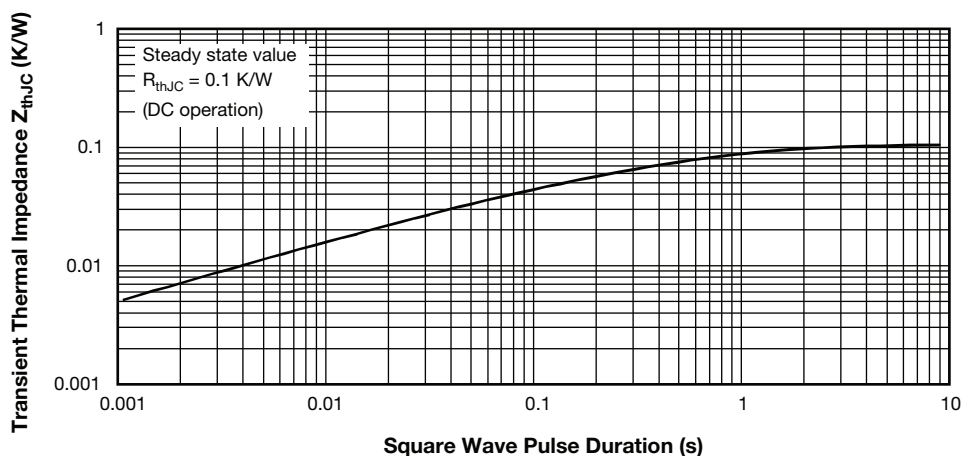


Fig. 7 - On-State Voltage Drop Characteristics

Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

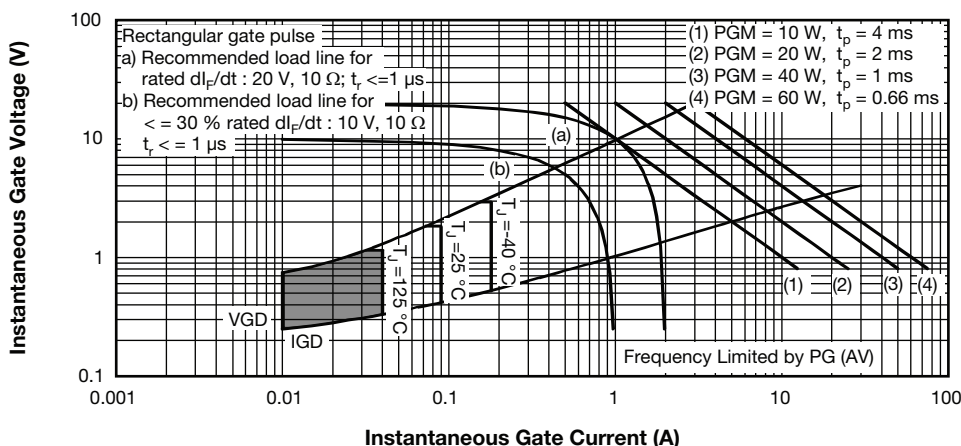


Fig. 9 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code	VS-	ST	23	0	S	12	P	0	V	PbF
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)

- 1** - Vishay Semiconductors product
- 2** - Thyristor
- 3** - Essential part number
- 4** - 0 = converter grade
- 5** - S = compression bonding stud
- 6** - Voltage code x 100 = V_{RRM} (see Voltage Ratings table)
- 7** - P = stud base 3/4"-16UNF2A threads
- 8** - 0 = eyelet terminals (gate and auxiliary cathode leads)
1 = fast-on terminals (gate and auxiliary cathode leads)
- 9** - V = glass-metal seal (only up to 1200 V)
- 10** - None = standard production
PbF = lead (Pb)-free

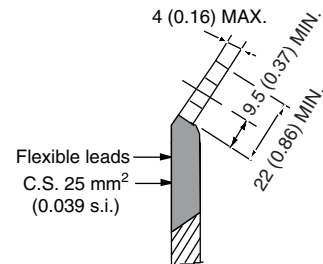
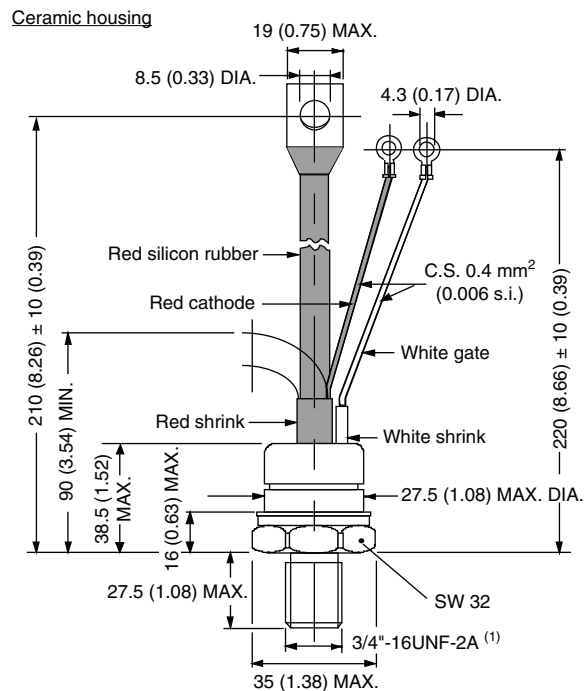
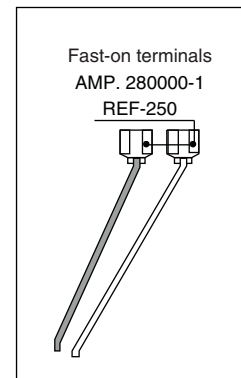
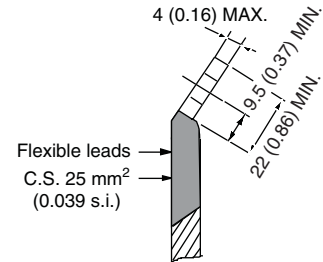
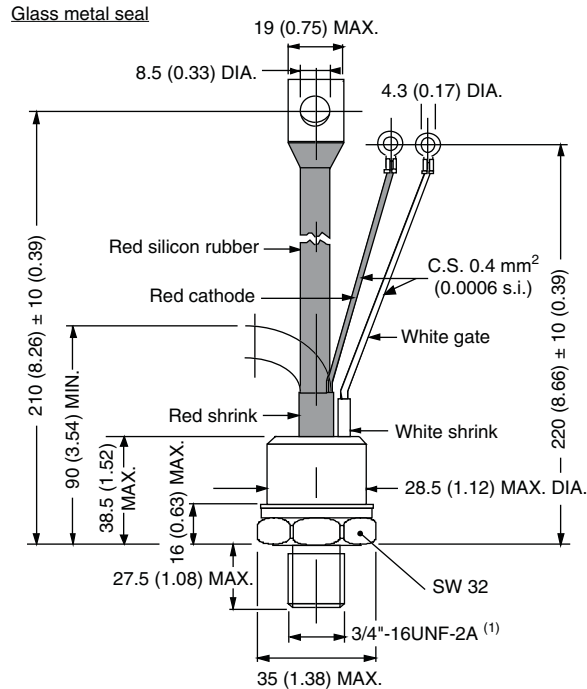
Note: For metric device M16 x 1.5 contact factory

LINKS TO RELATED DOCUMENTS

Dimensions	www.vishay.com/doc?95082
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TO-209AB (TO-93)

DIMENSIONS in millimeters (inches)



Note

(1) For metric device: M16 x 1.5 - length 21 (0.83) maximum



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