EMIPAK 1B PressFit Power Module 800 V Half Controlled Single Phase Bridge, 20 A 600 V PFC and Half Bridge MOSFET, 40 A

EMIPAK 1B (package example)

PRIMARY CHARACTERISTICS	
HALF CONTROLLED SINGLE PHASE BRIDGE	
I_O at T_{SINK} = 115 °C	20 A
D1, D2	
V_{RRM}	800 V
V_{FM} typical at 20 A	1.10 V
SCR1, SCR2	
V_{RRM}/V_{DRM}	800 V
V_{TM} typical at 20 A	1.29 V
QB1 - QB2 - QB3 MOSFET	
V_{DSS}	600 V
$R_{DS(on)}$ typical at I_C = 40 A	37 mΩ
I_D at T_{SINK} = 39 °C	40 A
D3 SILICON CARBIDE CLAMP DIODE	
V_{RRM}	600 V
V_{FM} typical at 30 A	1.72 V
I_F at T_C = 46 °C	30 A
Type	Modules - MOSFET
Package	EMIPAK 1B
Circuit configuration	Half controlled input bridge plus MOSFET boost PFC leg and MOSFET half bridge inverter

FEATURES

RoHS COMPLIANT

- E series power MOSFET with fast body diode
- MOAT and SiC diode technology
- Thyristor phase control
- Exposed Al_2O_3 substrate with low thermal resistance
- Low input capacitance
- Low switching and conduction losses
- Ultra low gate charge Q_g
- Low internal inductances
- Qualified using AQG324 guideline as reference
- PressFit pins locking technology
  PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION

The EMIPAK 1B package is easy to use thanks to the PressFit pins. The exposed substrate provides improved thermal performance.

The optimized layout also helps to minimize stray parameters, allowing for better EMI performance.

PATENT(S): www.vishay.com/patents
This Vishay product is protected by one or more United States and international patents.

ABSOLUTE MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MAX.**	**UNITS**
Operating junction temperature	T_J		150	°C
Storage temperature range	T_{Stg}		-40 to +150	
RMS isolation voltage	V_{ISOL}	T_J = 25 °C, all terminals shorted, f = 50 Hz, t = 1 s	3500	V
HALF CONTROLLED SINGLE PHASE BRIDGE				
Maximum DC output current of bridge	I_O	T_{SINK} = 25 °C	44	A
		T_{SINK} = 80 °C	31	
One-cycle non-repetitive on-state peak or forward current	I_{FSM}/I_{TSM}	10 ms sine or 6 ms rectangular pulse, T_J = 150 °C, no voltage reapplied	273	
Maximum I^2t for fusing	I^2t	10 ms sine pulse, no voltage reapplied	374	A^2s
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied	3740	$A^2\sqrt{s}$
Value of threshold voltage	$V_{F(TO)}$	T_J = 150 °C	1.04	V
Slope resistance	r_t	T_J = 150 °C	38.9	mΩ
Repetitive peak reverse diode	V_{RRM}		800	V
Repetitive peak direct and reverse thyristor	V_{RRM}/V_{DRM}		800	V
Maximum critical rate of rise of off-state voltage - thyristor	dV/dt	V_{DRM} = 80 % of rated voltage, T_J = 125 °C	500	V/µs
Maximum non-repetitive rate of rise of turned on current - thyristor	dI/dt	T_J = 125 °C	150	A/µs
QB1 - QB2 - QB3 MOSFET				
Drain to source voltage	V_{DSS}		600	V
Gate to source voltage	V_{GS}		± 30	
Pulsed drain current	I_{DM}	V_{GS} = 10 V	135	A
Continuous drain current	I_D	T_{SINK} = 25 °C	42	A
		T_{SINK} = 80 °C	32	
Power dissipation	P_D	T_{SINK} = 25 °C	174	W
		T_{SINK} = 80 °C	97	
Single pulse avalanche energy	E_{AS}	L = 10 mH, I_{AS} = 23 A, T_J = 25 °C	2645	mJ
Pulsed source current (body diode)	I_{SM}		135	A
D3 SILICON CARBIDE CLAMP DIODE				
Cathode to anode voltage	V_{RRM}		600	V
Single pulse forward current	I_{FSM}	10 ms sine or 6 ms rectangular pulse, T_J = 25 °C	234	A
Diode continuous forward current	I_F	T_{SINK} = 25 °C	33	A
		T_{SINK} = 80 °C	23	
Power dissipation	P_D	T_{SINK} = 25 °C	96	W
		T_{SINK} = 80 °C	54	

ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
INPUT SINGLE PHASE BRIDGE						
D1, D2						
Forward voltage drop	V_{FM}	I_F = 20 A	-	1.10	1.32	V
		I_F = 20 A, T_J = 150°C	-	1.02	-	
Breakdown voltage	V_{BR}	I_R = 500 μA	800	-	-	V
Reverse leakage current	I_{RM}	V_R = 800 V	-	0.7	100	μA
		V_R = 800 V, T_J = 150 °C	-	0.7	-	mA
SCR1, SCR2						
Peak on state voltage	V_{TM}	I_{TM} = 20 A	-	1.29	1.70	V
		I_{TM} = 20 A, T_J = 150 °C	-	1.24	-	
Breakdown voltage	V_{RRM}/V_{DRM}	I_R = 500 μA	800	-	-	V
Reverse and direct leakage current	I_{RM}/I_{DM}	V_R = 800 V	-	1.0	100	μA
		V_R = 800 V, T_J = 150°C	-	4.5	-	mA
QB1 - QB2 - QB3 MOSFET						
Drain to source breakdown voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	600	-	-	mΩ
Drain to source on resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 40 A	-	37	48	
		V_{GS} = 10 V, I_D = 40 A, T_J = 150 °C	-	87	-	
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.8	2.7	4.4	V
Temperature coefficient of threshold voltage	$\Delta V_{GS(th)}/\Delta T_J$	V_{DS} = V_{GS}, I_D = 250 μA (25 °C to 125 °C)	-	-11.4	-	mV/°C
Forward transconductance	g_{fs}	V_{DS} = 20 V, I_D = 40 A	-	48	-	S
Transfer characteristics	V_{GS}	V_{DS} = 20 V, I_D = 40 A	-	5.3	-	V
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 600 V	-	0.7	10	μA
		V_{GS} = 0 V, V_{DS} = 600 V, T_J = 150 °C	-	1.1	-	mA
Gate to source leakage current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0 V	-	-	± 150	nA
QB1 - QB2 - QB3 MOSFET BODY DIODE						
Source-to-drain voltage drop	V_{SD}	I_{SD} = 40 A, V_{GS} = 0 V	-	0.92	1.32	V
D3 SILICON CARBIDE CLAMP DIODE						
Forward voltage drop	V_{FM}	I_F = 30 A	-	1.72	1.98	V
		I_F = 30 A, T_J = 150 °C	-	2.37	-	
Breakdown voltage	V_{BR}	I_R = 1.5 mA	600	-	-	V
Reverse leakage current	I_{RM}	V_R = 600 V	-	0.6	300	μA
		V_R = 600 V, T_J = 150 °C	-	4.2	-	

TRIGGERING (T_J = 25 °C unless otherwise noted)				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
SCR1, SCR2				
Maximum peak gate power	P_{GM}		8.0	W
Maximum average gate power	$P_{G(AV)}$		2.0	W
Maximum peak gate current	I_{GM}		1.5	A
Maximum peak negative gate voltage	V_{GM}		10	V
Maximum gate voltage required to trigger	V_{GT}	T_J = 25 °C, anode supply = 6 V resistive load	2.0	V
		T_J = 125 °C, anode supply = 6 V resistive load	0.75	
Maximum gate current required to trigger	I_{GT}	T_J = 25 °C, anode supply = 6 V resistive load	45	mA
		T_J = 125 °C, anode supply = 6 V resistive load	14	
Maximum gate voltage that will not trigger	V_{GD}	T_J = 125 °C, 100 % V_{DRM} applied	0.2	V
Maximum gate current that will not trigger	I_{GD}	T_J = 125 °C, 100 % V_{DRM} applied	1.0	mA

SWITCHING (T_J = 25 °C unless otherwise noted)				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
SCR1, SCR2				
Typical turn-on time	t_{gt}	T_J = 25 °C	0.9	μs
Typical reverse recovery time	t_{rr}	T_J = 125 °C	4	
Typical turn-off time	t_g	T_J = 125 °C	110	

SWITCHING CHARACTERISTICS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
QB1 MOSFET with D3 CLAMP DIODE						
Total gate charge (turn-on)	Q_g	I_D = 32 A, V_{DS} = 480 V, V_{GS} = 10 V	-	240	-	nC
Gate to source charge (turn-on)	Q_{gs}		-	58	-	
Gate to drain charge (turn-on)	Q_{gd}		-	96	-	
Turn-on switching loss	E_{ON}	I_D = 40 A, V_{DD} = 450 V, V_{GS} = +10 V / -10 V, R_g = 10 Ω, L = 500 μH	-	0.53	-	mJ
Turn-on delay time	$t_{d(on)}$		-	43	-	ns
Rise time	t_r		-	26	-	
Turn-off switching loss	E_{OFF}		-	0.19	-	mJ
Turn-off delay time	$t_{d(off)}$		-	160	-	ns
Fall time	t_f		-	18	-	
Turn-on switching loss	E_{ON}	I_D = 40 A, V_{DD} = 450 V, V_{GS} = +10 V / -10 V, R_g = 10 Ω, L = 500 μH, T_J = 125 °C	-	0.63	-	mJ
Turn-on delay time	$t_{d(on)}$		-	39	-	ns
Rise time	t_r		-	29	-	
Turn-off switching loss	E_{OFF}		-	0.23	-	mJ
Turn-off delay time	$t_{d(off)}$		-	162	-	ns
Fall time	t_f		-	19	-	
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	7500	-	pF
Output capacitance	C_{oss}		-	378	-	
Reverse transfer capacitance	C_{rss}		-	5	-	
Reverse bias safe operating area	RBSOA	T_J = 150 °C, I_D = 100 A, V_{DD} = 400 V, V_P = 600 V, R_g = 10 Ω, V_{GS} = +10 V / 0 V				
QB2 - QB3 MOSFET						
Total gate charge (turn-on)	Q_g	I_D = 32 A, V_{DS} = 480 V, V_{GS} = 10 V	-	240	-	nC
Gate-source charge	Q_{gs}		-	58	-	
Gate-drain charge	Q_{gd}		-	96	-	
Turn-off switching loss	E_{OFF}	I_D = 40 A, V_{DD} = 450 V, V_{GS} = +10 V / -10 V, R_g = 10 Ω, L = 500 μH	-	0.17	-	mJ
Turn-off delay time	$t_{d(off)}$		-	157	-	ns
Fall time	t_f		-	18	-	
Turn-off switching loss	E_{OFF}	I_D = 40 A, V_{DD} = 450 V, V_{GS} = +10 V / -10 V, R_g = 10 Ω, L = 500 μH, T_J = 125 °C	-	0.19	-	mJ
Turn-off delay time	$t_{d(off)}$		-	164	-	ns
Fall time	t_f		-	19	-	
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	7500	-	pF
Output capacitance	C_{oss}		-	378	-	
Reverse transfer capacitance	C_{rss}		-	5	-	
Reverse bias safe operating area	RBSOA	T_J = 150 °C, I_D = 150 A, V_{DD} = 400 V, V_P = 600 V, R_g = 10 Ω, V_{GS} = +10 V / 0 V				
QB1 - QB2 - QB3 MOSFET BODY DIODE						
Diode reverse recovery time	t_{rr}	V_R = 200 V, T_J = 25 °C, I_S = 40 A, dI/dt = 100 A/μs	-	211	-	ns
Diode reverse recovery current	I_{rr}		-	17	-	A
Diode reverse recovery charge	Q_{rr}		-	1775	-	nC
D3 SILICON CARBIDE CLAMP DIODE						
Total capacitive charge	Q_C	V_R = 600 V, I_F = 30 A, dI/dt = 500 A/μs	-	75	-	nC

INTERNAL NTC - THERMISTOR SPECIFICATIONS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUE**	**UNITS**
Resistance	R25	T_C = 25 °C	5000	Ω
	R100	T_C = 100 °C	493 ± 5 %	
B-value	$B_{25/50}$	$R_2 = R_{25}$ exp. $[B_{25/50}(1/T2 - 1/(298.15K))]$	3375 ± 5 %	K
Maximum operating temperature			220	°C
Dissipation constant			2	mW/°C
Thermal time constant			8	s

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
INPUT SINGLE PHASE BRIDGE - Junction to sink thermal resistance (per diode) [(1)]	R_{thJS}	-	1.28	-	°C/W
INPUT SINGLE PHASE BRIDGE - Junction to sink thermal resistance (per thyristor) [(1)]		-	1.11	-	
QB1 - QB2 - QB3 MOSFET - Junction to sink thermal resistance (per switch) [(1)]		-	0.64	-	
D3 SILICON CARBIDE CLAMP DIODE - Junction to sink thermal resistance (per diode) [(1)]		-	1.07	-	
Case to sink thermal resistance (per module) [(1)]		-	0.1	-	
Mounting torque (M4)		2	-	3	Nm
Weight		-	28	-	g

Note

(1) Mounting surface flat, smooth, and greased, λ_{grease} = 0.67 W/mK

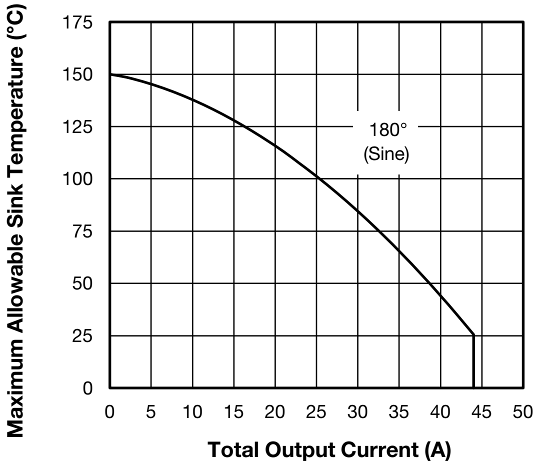


Fig. 1 - Current Rating Characteristics

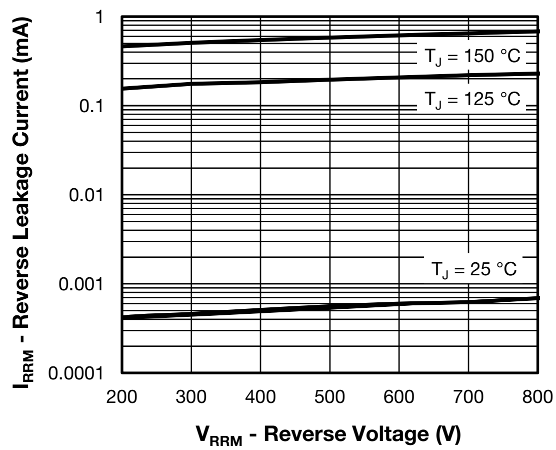


Fig. 4 - Typical D1 - D2 Reverse Current vs. Reverse Voltage

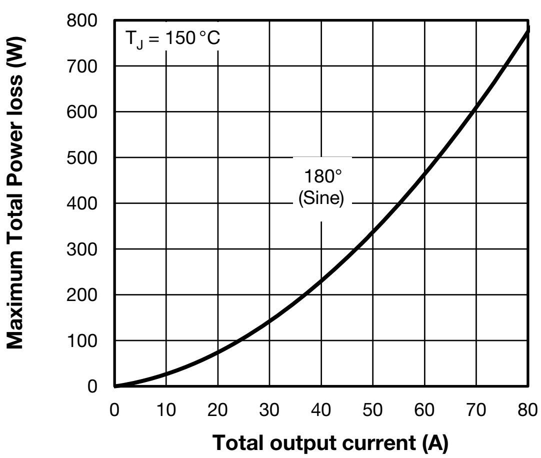


Fig. 2 - Total Power Loss Characteristics

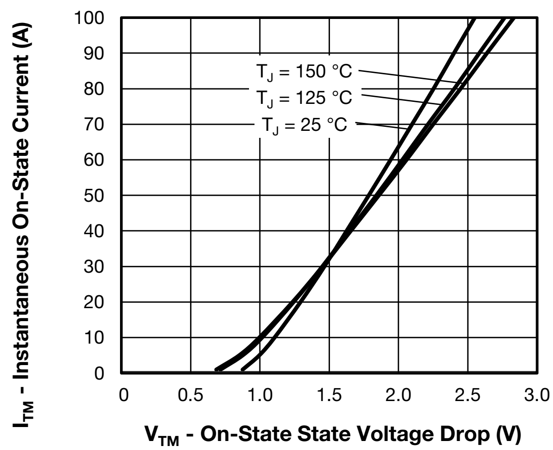


Fig. 5 - Typical Scr1 - Scr2 On-State Voltage Drop vs. Instantaneous On-State Current

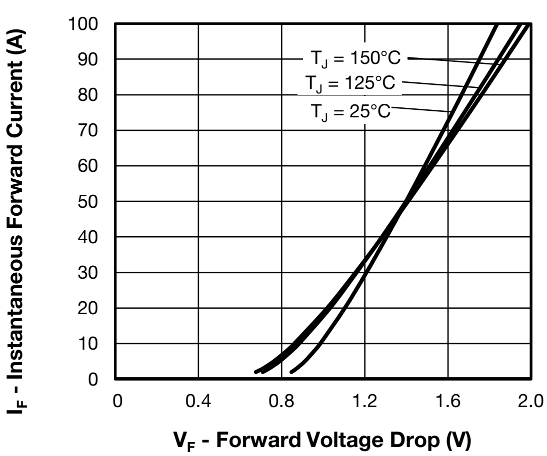


Fig. 3 - Typical D1 - D2 Forward Voltage Drop vs. Instantaneous Forward Current

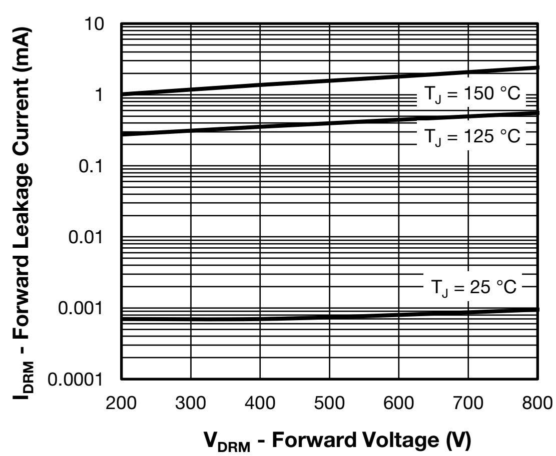


Fig. 6 - Typical Scr1 - Scr2 Forward Leakage Current vs. Direct Blocking Voltage

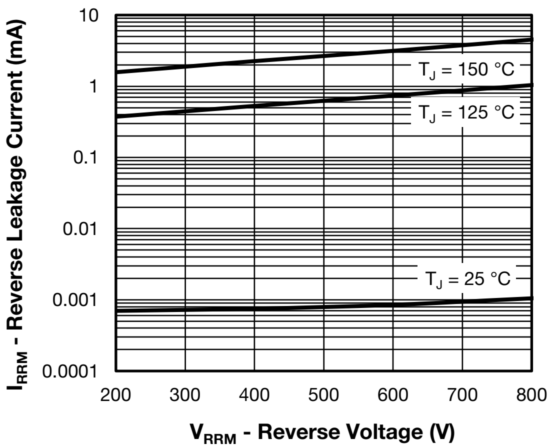


Fig. 7 - Typical Scr1 - Scr2 Reverse Leakage Current vs. Reverse Blocking Voltage

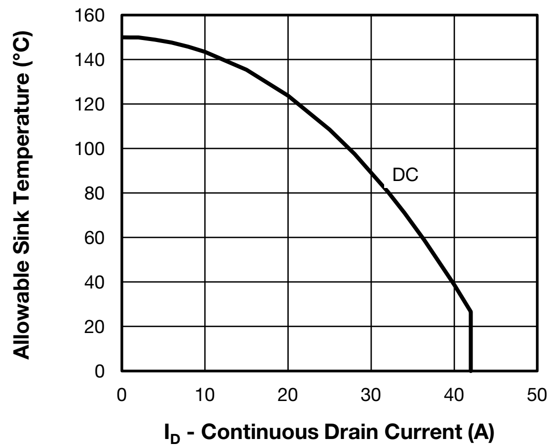


Fig. 10 - Maximum QB1 - QB3 Continuous Drain Current vs. Sink Temperature

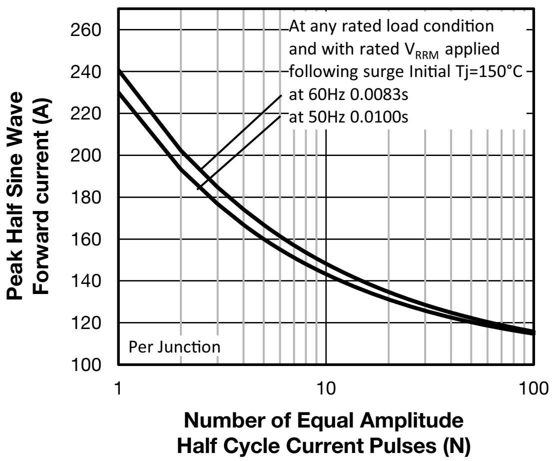


Fig. 8 - Maximum Non-Repetitive Surge Current vs. Number of Current Pulses

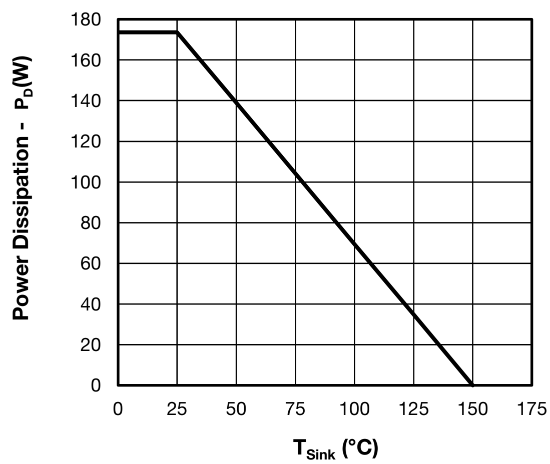


Fig. 11 - QB1 - QB3 Power Dissipation Curve

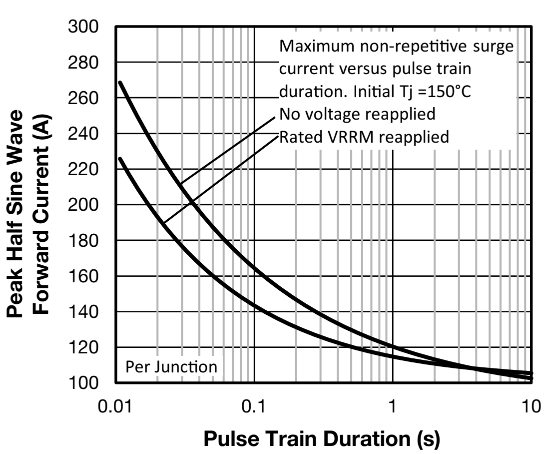


Fig. 9 - Maximum Non-Repetitive Surge Current vs. Pulse Train Duration

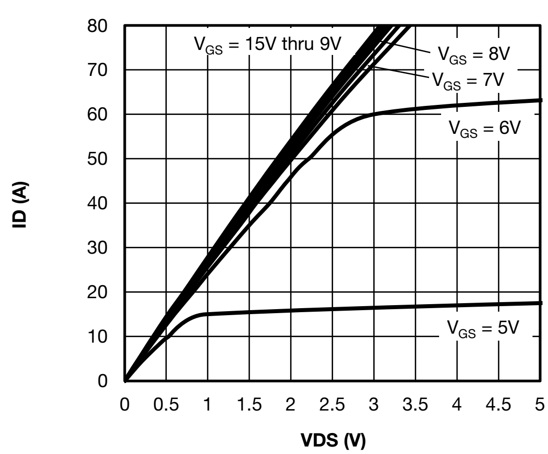


Fig. 12 - Typical QB1 - QB3 Drain to Source Current Output Characteristics at T_J = 25 °C

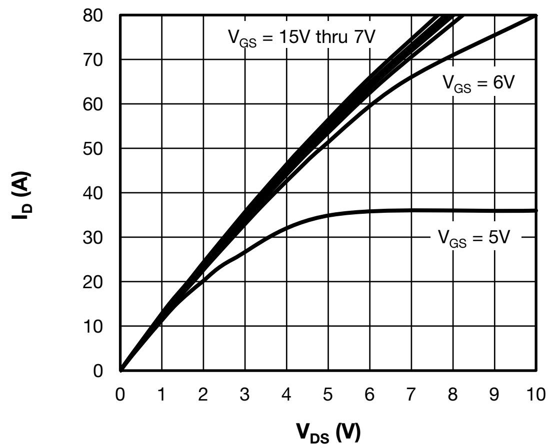


Fig. 13 - Typical QB1 - QB3
Drain to Source Current Output Characteristics at T_J = 150 °C

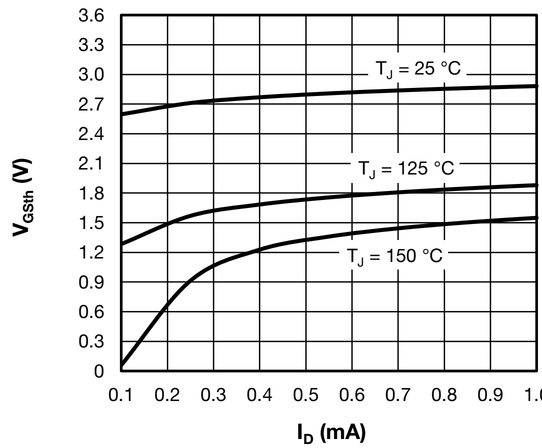


Fig. 16 - Typical QB1-QB3
Gate Threshold Voltage Characteristics

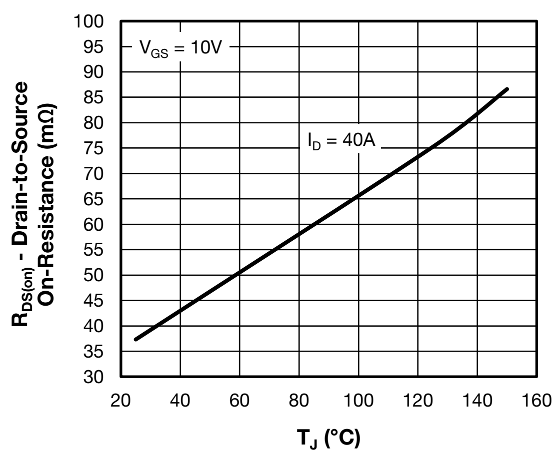


Fig. 14 - Typical QB1 - QB3
Drain-to-Source On-Resistance vs. Temperature

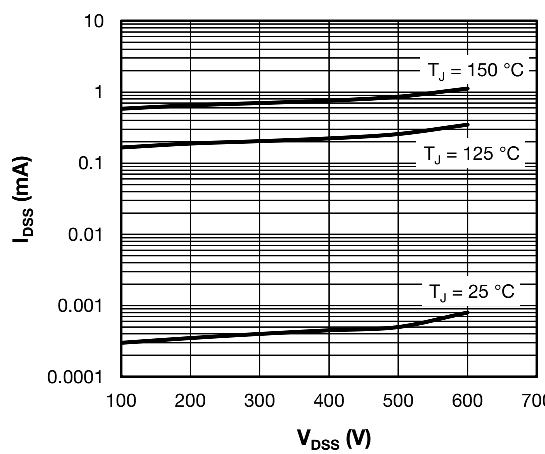


Fig. 17 - Typical QB1 - QB3
Zero Gate Voltage Drain Current

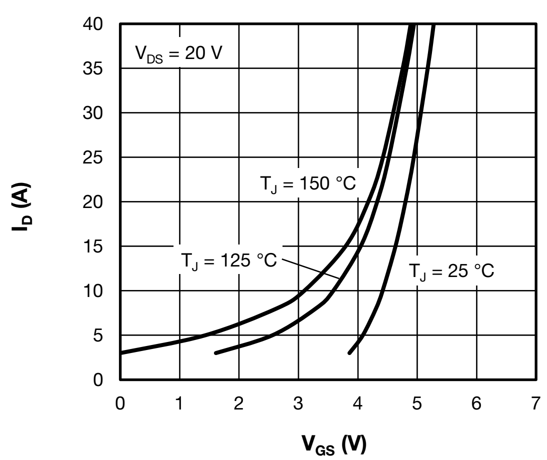


Fig. 15 - Typical QB1 - QB3
Transfer Characteristics

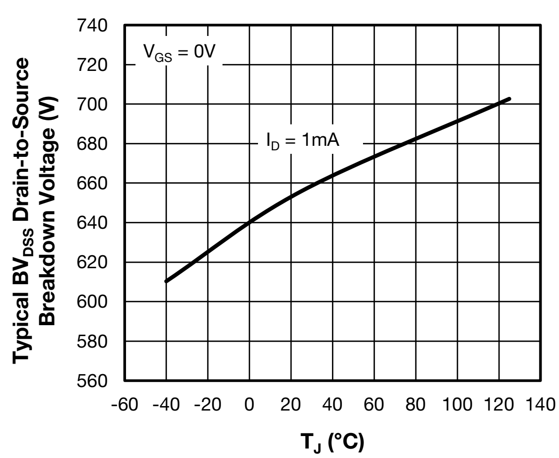


Fig. 18 - Typical QB1 - QB3
Drain to Source Breakdown Voltage vs. Temperature

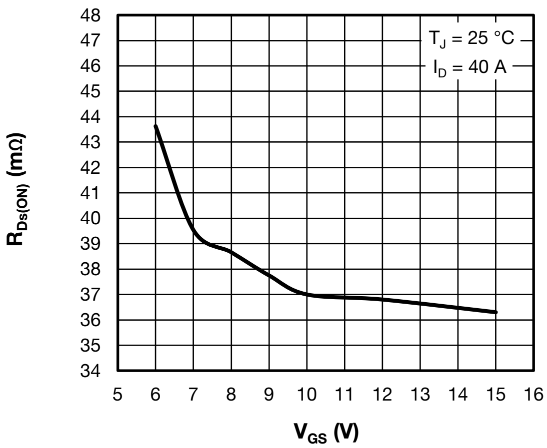


Fig. 19 - Typical QB1 - QB3
Drain - State Resistance vs. Gate-to-Source Voltage

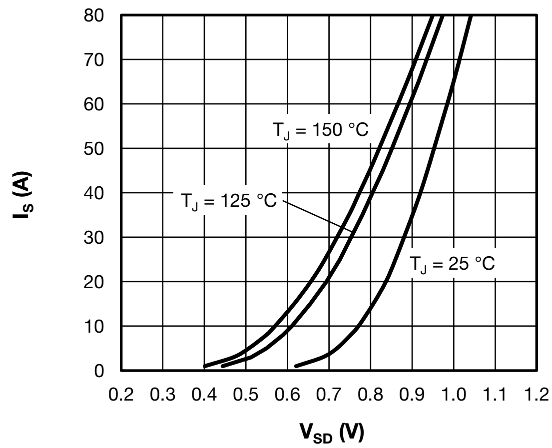


Fig. 22 - Typical QB1 - QB3
Body Diode Source-to-Drain Current Characteristics

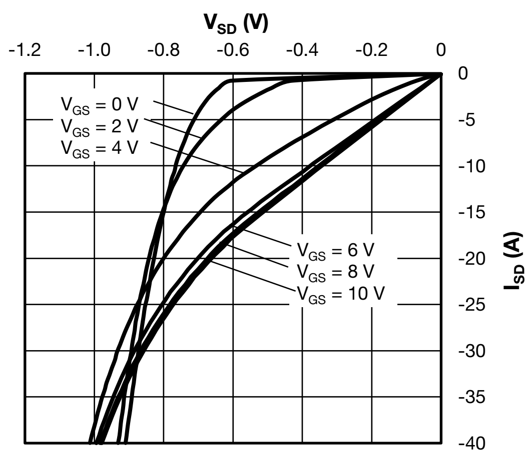


Fig. 20 - Typical QB1 - QB3
Source-to-Drain Current Characteristics at T_J = 125 °C

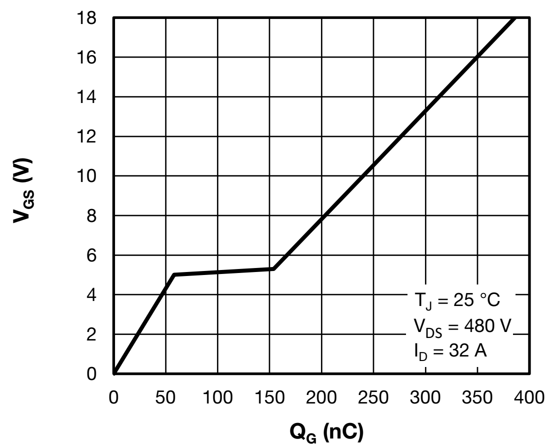


Fig. 23 - Typical QB1 - QB3
Gate charge vs. Gate-to-Source Voltage

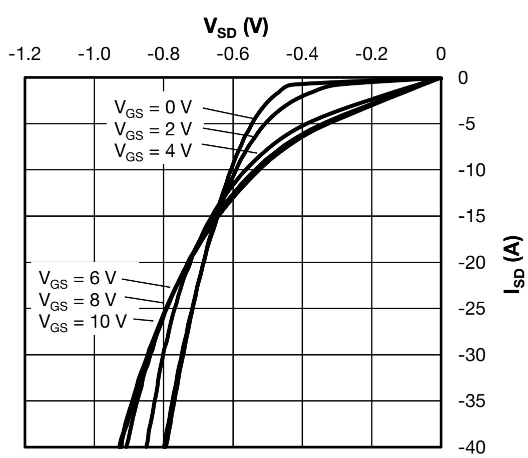


Fig. 21 - Typical QB1 - QB3
Source-to-Drain Current Characteristics at T_J = 125 °C

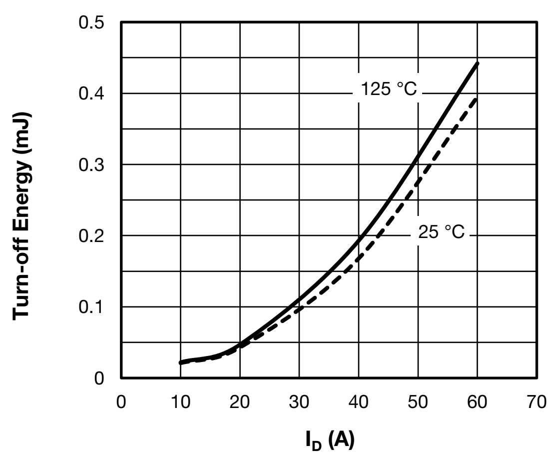


Fig. 24 - Typical QB2 - QB3 Turn-off Energy Loss vs. I_D
V_{DD} = 450 V, R_g = 10 Ω, V_{GS} = ± 10 V, L = 500 μH

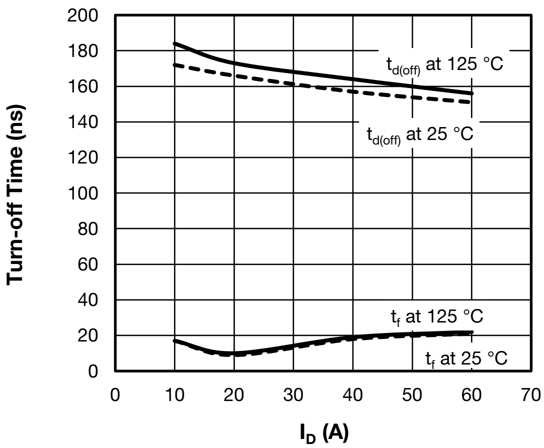


Fig. 25 - Typical QB2-QB3 Turn-off Switching Time vs I_D
V_{DD} = 450 V, R_g = 10 Ω, V_{GS} = ± 10 V, L = 500 μH

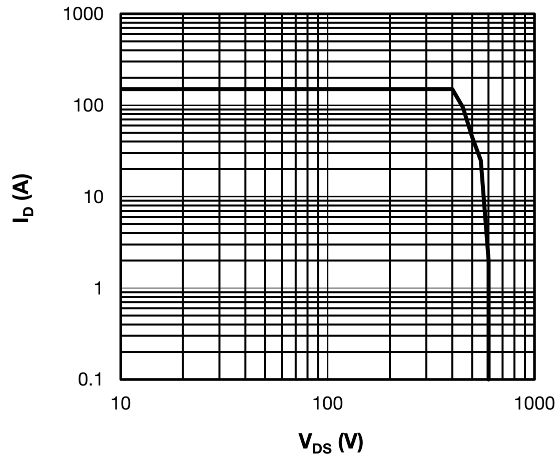


Fig. 28 - QB2 - QB3 MOSFET Reverse BIAS SOA
T_J = 150 °C, V_{GS} = 10 V

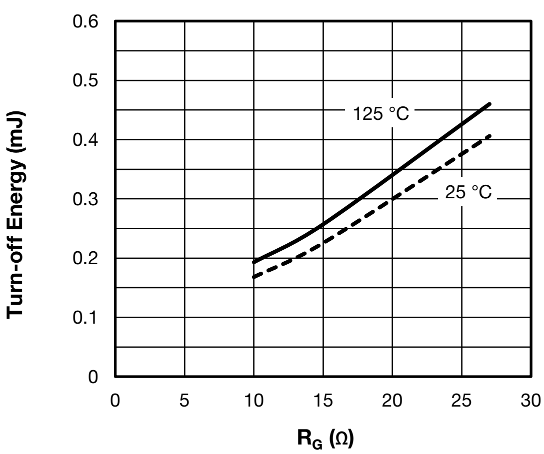


Fig. 26 - Typical QB2-QB3 Turn-off Energy Loss vs Rg
V_{DD} = 450 V, I_D = 40 A, V_{GS} = ± 10 V, L = 500 μH

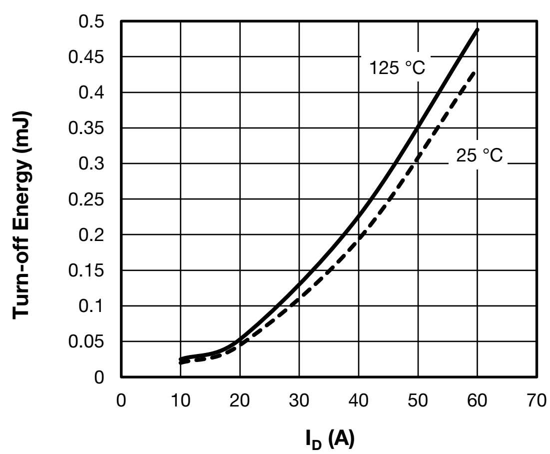


Fig. 29 - Typical QB1 Turn-off Energy Loss vs. I_D
V_{DD} = 450 V, R_g = 10 Ω, V_{GS} = ± 10 V, L = 500 μH

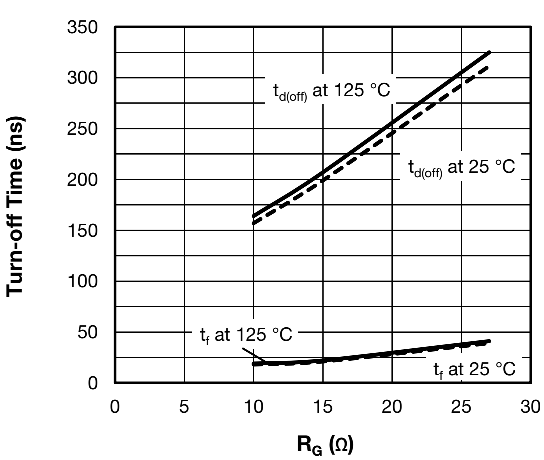


Fig. 27 - Typical QB2-QB3 Turn-off Switching Time vs Rg
V_{DD} = 450 V, I_D = 40 A, V_{GS} = ± 10 V, L = 500 μH

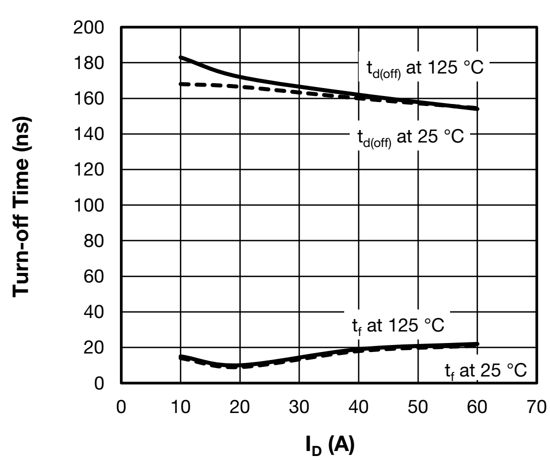


Fig. 30 - Typical QB1 Turn-off Switching Time vs. I_D
V_{DD} = 450 V, R_g = 10 Ω, V_{GS} = ± 10 V, L = 500 μH

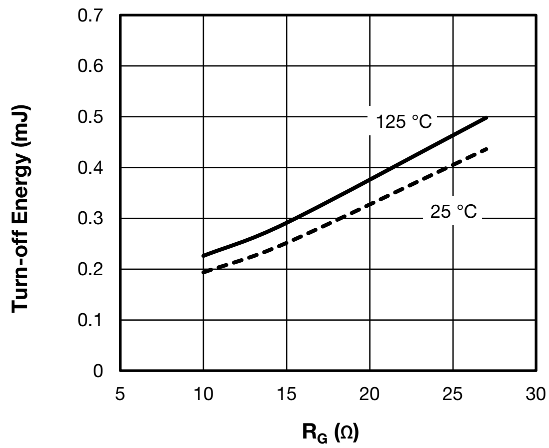


Fig. 31 - Typical QB1 Turn-off Energy Loss vs. R_g
V_{DD} = 450 V, I_D = 40 A, V_{GS} = ± 10 V, L = 500 µH

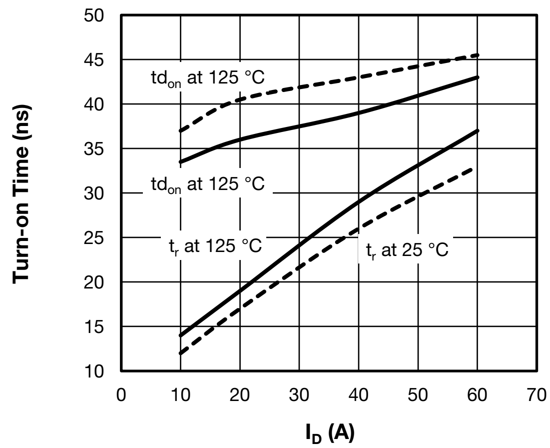


Fig. 34 - Typical QB1 Turn-on Switching Time vs. I_D
V_{DD} = 450 V, R_g = 10 Ω, V_{GS} = ± 10 V, L = 500 µH

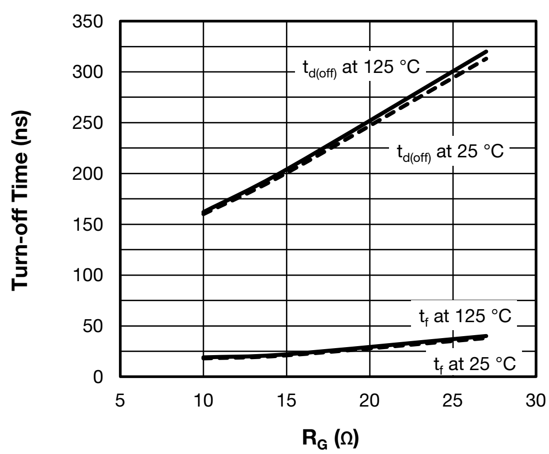


Fig. 32 - Typical QB1 Turn-off Switching Time vs. R_g
V_{DD} = 450 V, I_D = 40 A, V_{GS} = ± 10 V, L = 500 µH

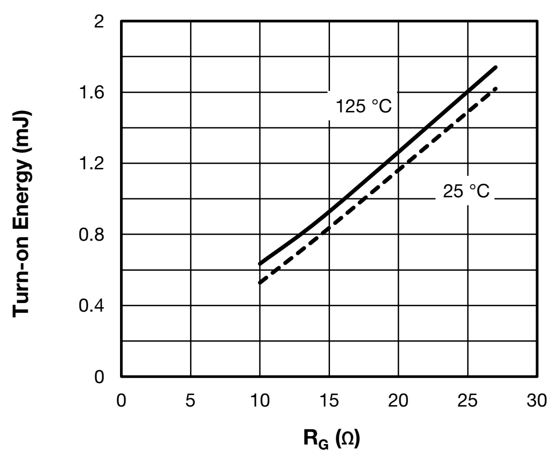


Fig. 35 - Typical QB1 Turn-on Energy Loss vs. R_g
V_{DD} = 450 V, I_D = 40 A, V_{GS} = ± 10 V, L = 500 µH

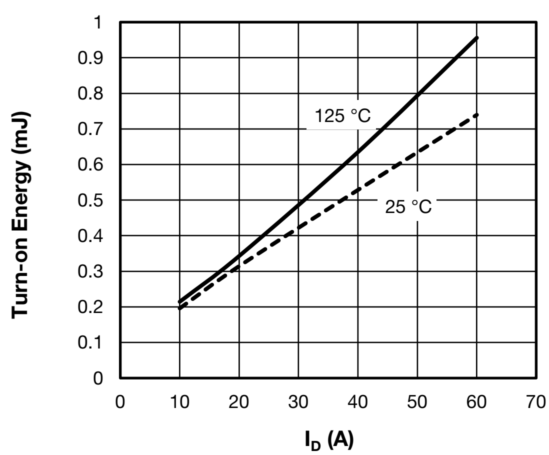


Fig. 33 - Typical QB1 Turn-on Energy Loss vs. I_D
V_{DD} = 450 V, R_g = 10 Ω, V_{GS} = ± 10 V, L = 500 µH

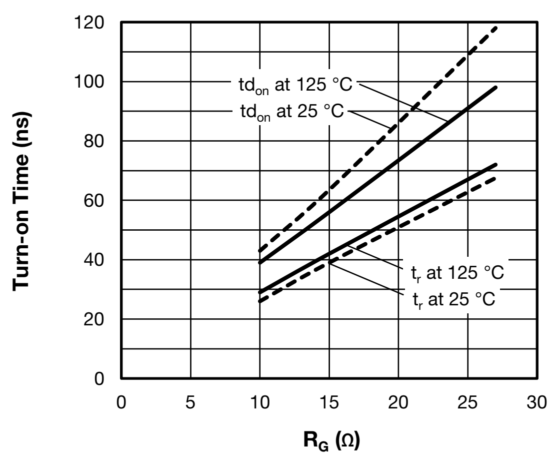


Fig. 36 - Typical QB1 Turn-on Switching Time vs. R_g
V_{DD} = 450 V, I_D = 40 A, V_{GS} = ± 10 V, L = 500 µH

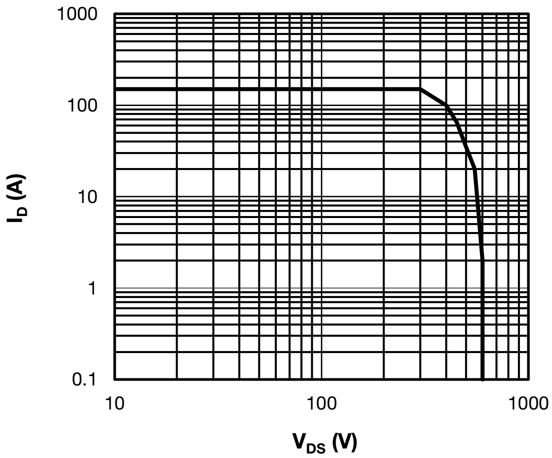


Fig. 37 - QB1 MOSFET Reverse BIAS SOA
T_J = 150 °C, V_{GS} = 10 V

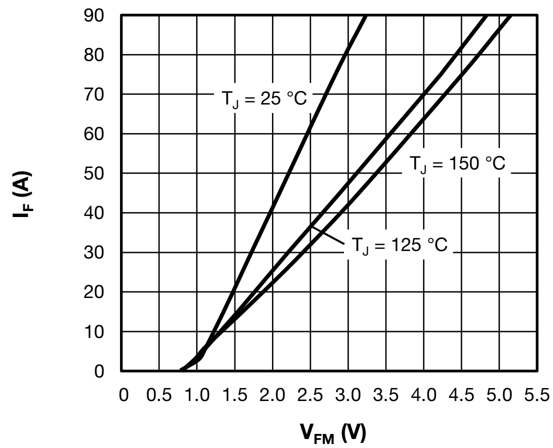


Fig. 39 - Typical D3 Diode Forward Characteristics

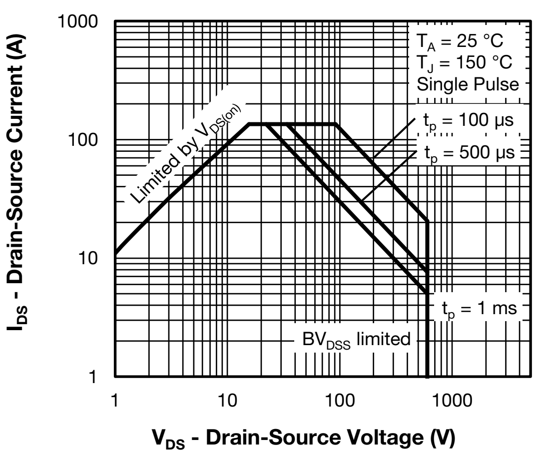


Fig. 38 - QB1 - QB3 Safe Operating Area

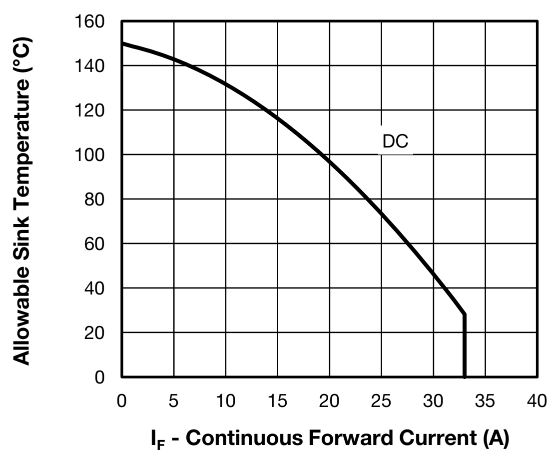


Fig. 40 - Maximum D3 Diode Continuous Forward Current vs. Sink Temperature

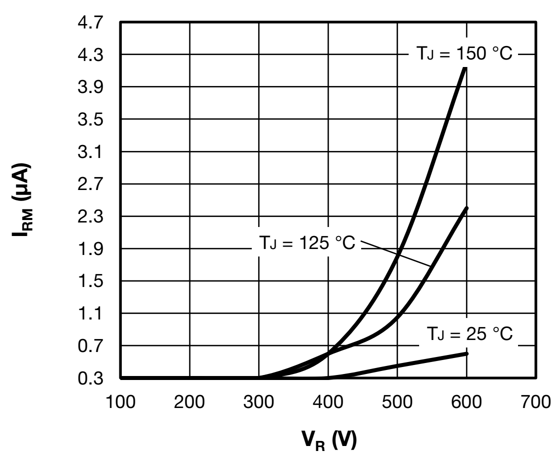


Fig. 41 - Typical D3 Diode Reverse Leakage Current

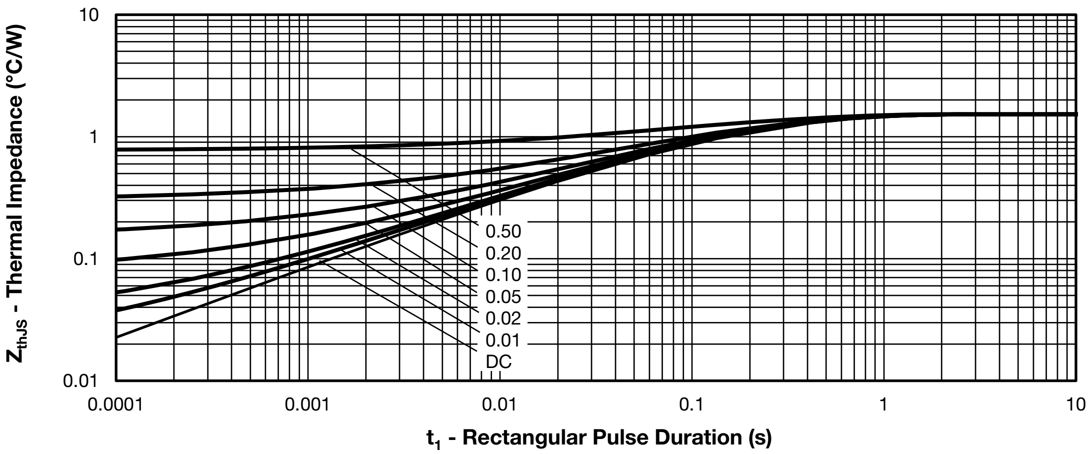


Fig. 42 - Maximum D1 - D2 Z_{thJS} Thermal Impedance Characteristic

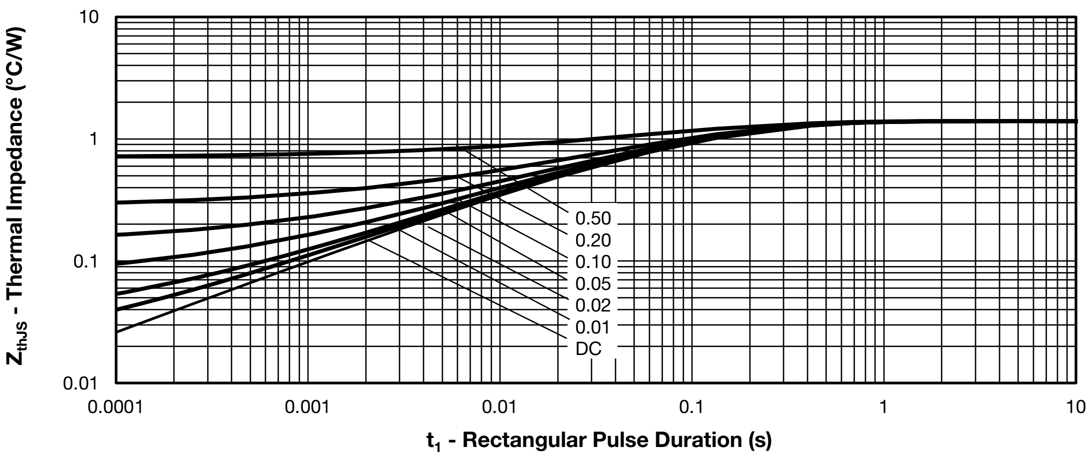


Fig. 43 - Maximum Scr1 - Scr2 Z_{thJS} Thermal Impedance Characteristic

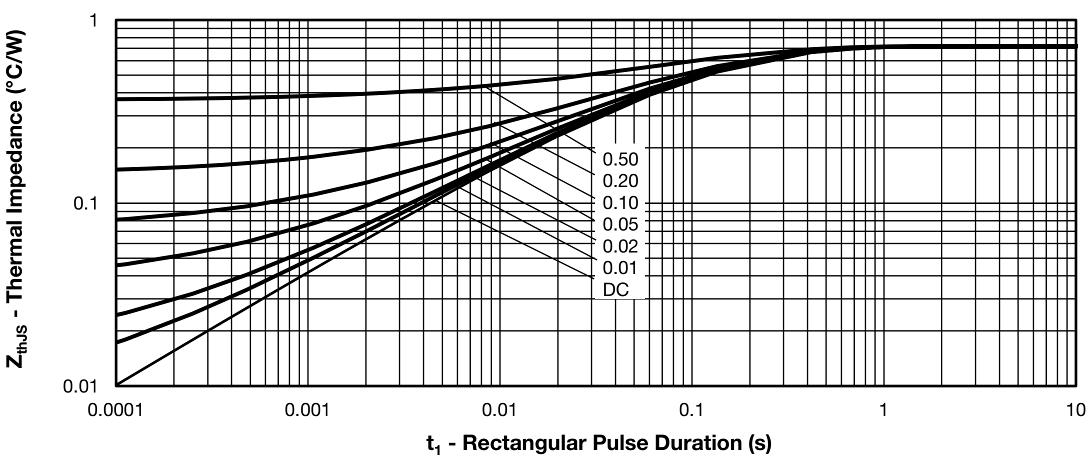


Fig. 44 - Maximum QB1 - QB3 Z_{thJS} Thermal Impedance Characteristic

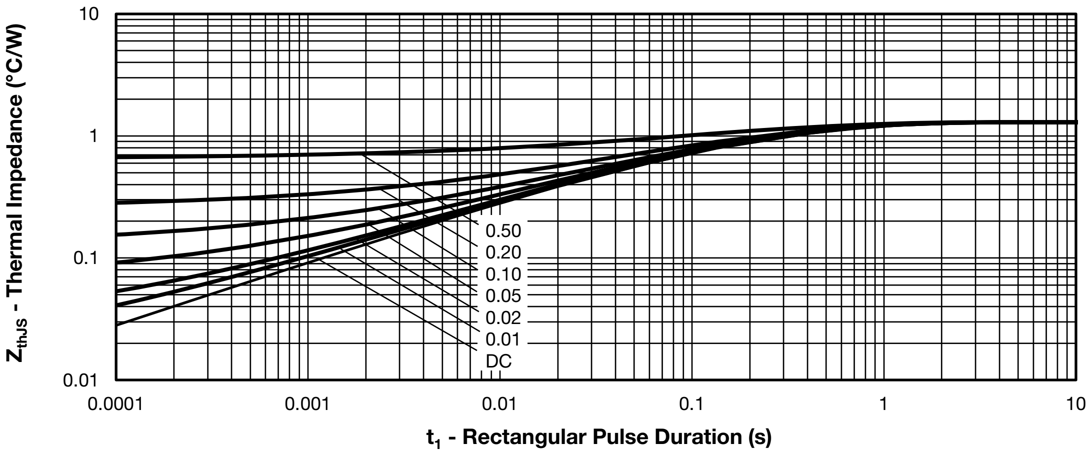


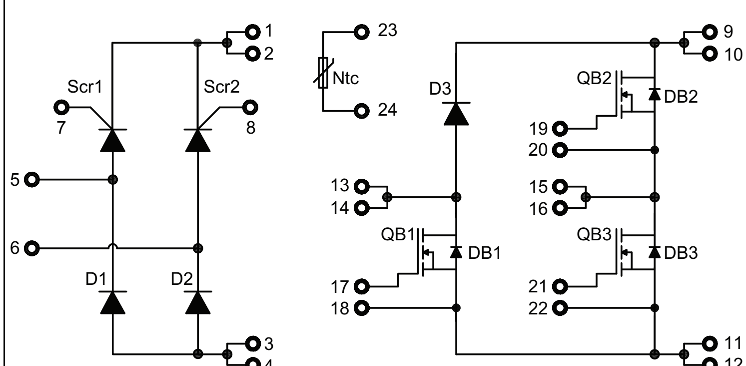
Fig. 45 - Maximum D3 Z_{thJS} Thermal Impedance Characteristics

ORDERING INFORMATION TABLE

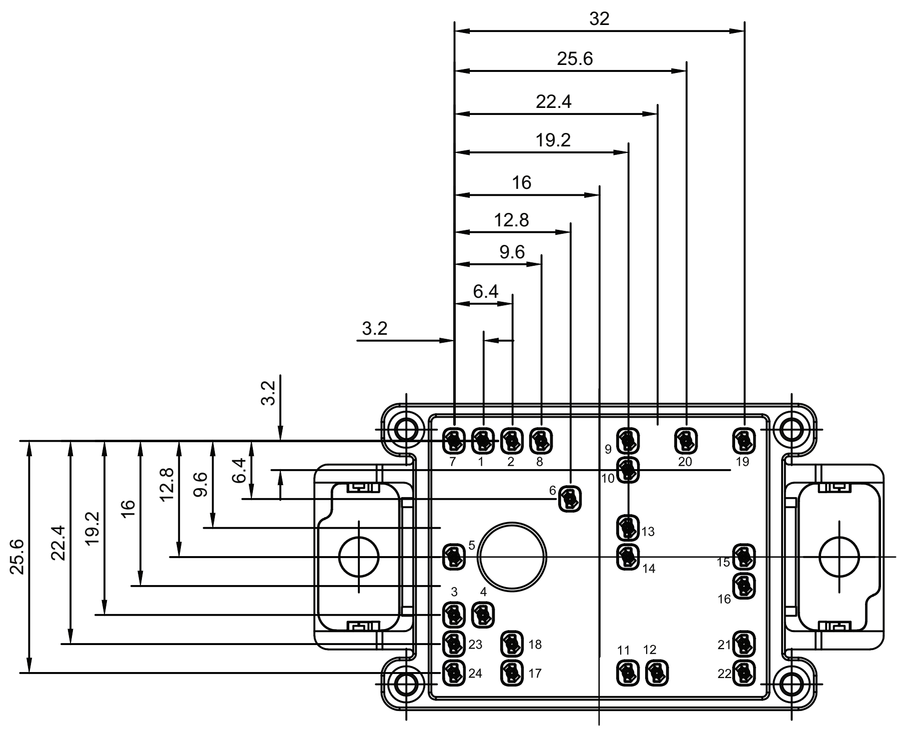
Device code

VS-	EN	M	040	M	60	P
1	2	3	4	5	6	7

1	-	Vishay Semiconductors product
2	-	Package indicator (EN = EMIPAK 1B)
3	-	Circuit configuration (M = Half controlled input bridge plus MOSFET boost PFC leg and MOSFET half bridge inverter)
4	-	Current rating (040 = 40 A)
5	-	Switch die technology (M = SiC diodes + Power MOSFET + MOAT)
6	-	Voltage rating (60 = 600 V)
7	-	Diode technology (P = SiC diodes + MOAT + SCR)

CIRCUIT CONFIGURATION		
CIRCUIT	**CIRCUIT CONFIGURATION CODE**	**CIRCUIT DRAWING**
Half controlled input bridge plus MOSFET boost PFC leg and MOSFET half bridge inverter	M	

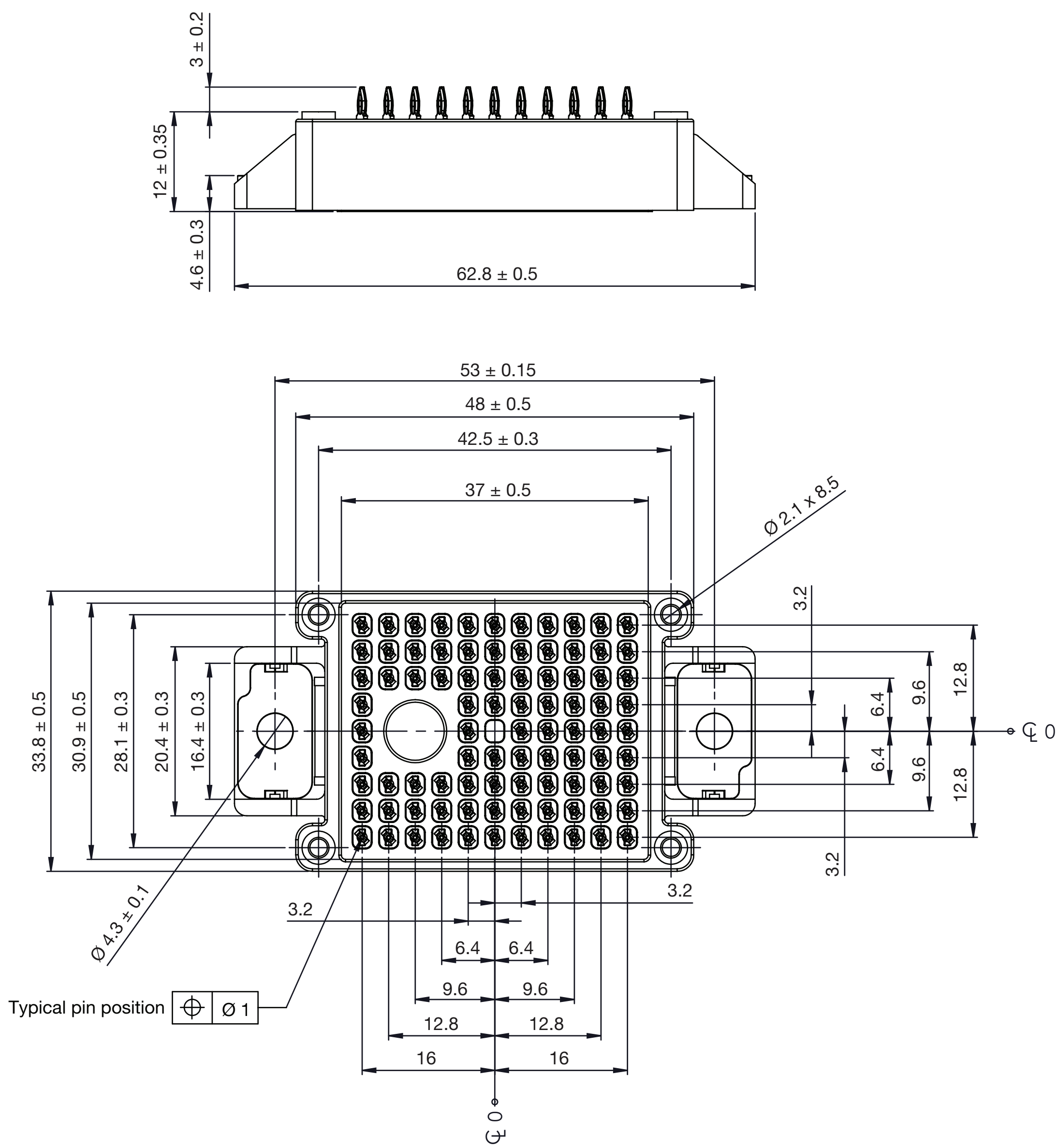
PACKAGE



LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95558
Application Note	www.vishay.com/doc?95580

EMIPAK-1B PressFit

DIMENSIONS in millimeters



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