SPICE Device Model VS-E7MH0112-M3, VS-E7MH0112HM3

Vishay Semiconductors

Si Ultrafast Diode 1 A, 1200 V

DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of diode. The models are extracted and optimized at junction temperature of 25 °C and can be used at 125 °C with temp. parameter removing V_p parameter.

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Vp parameter works only with LTspice[®] and describe the real softness of diode other simulator usually has not this capability. Currently the model is electrical only. Thermal model is available as RC model but is only to evaluate junction temperature. The electrical characteristics are independent from junction temperature of thermal model.

The model could be used as general spice model 3f5 compliant removing $V_{\rm p}$ parameter

All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device. The forward voltage is accurate until 10 times the rated current.

Reverse leakage currents are modelled in the range of μ A like the maximum value in the datasheet at the breakdown voltage instead of nA as the real device this to simplify the convergence of simulation.

The reverse recovery cannot be completely simulated from spice. The model give a limited information about switching losses.

ELECTRICAL

- + IS=5.0000E-6
- + N=3.7808
- + RS=65.513E-3
- + IKF=.40226
- + CJO=14.055E-12
- + M=.19493
- + VJ=.2
- + ISR=10.010E-21
- + NR=4.9950
- + BV=1.345E3
- + IBV= 0.1
- *use follow TT for spide3f5 compliant simulator or other Tj simulation *+ TT=44.658E-9
- + XTI=16
- + Tikf=0.066
- + Trs1=0.0025
- *use follow TT an Vp with LTspice at 25°C
- + TT=145.658E-9

CHARACTERISTICS

- · Si ultrafast pin diode
- Models optimized for T_J 25 °C and T_J 125 °C
- Isothermal electric characteristic
- Accurate conduction losses evaluation
- · Separate RC thermal model
- Model does not include the stray inductance and parasitic capacitance of package
- For SMA add in series 2.1 nH for device assembled with return path off current under the device
- Parasitic capacitance for SMA soldered on minimum pad size is 0.8 pF and could be considered concentrate in parallel at the diode for recommended footprint on FR4 substrate
- Add package parasitic could increase a lot the computing time
- Parasitic element could be different from above value and are related at layout
- In the subcircuit of thermal model the Z_{th} is referred at solder point. The T_a "ambient" temperature is the temperature of solder point. To complete the model of assembled part model of PCB should be added at knot T_a

THERMAL

.SUBCKT ZTH-VS-E7MH0112 Tj Ta

RTHERM1 Tj 1 1.588e-01 RTHERM2 1 2 1.249e+00 RTHERM3 2 3 6.286e+00 RTHERM4 3 Ta 8.185e+00

CTHERM1 T_j 1 2.136e-05 CTHERM2 1 2 3.573e-04 CTHERM3 2 3 4.023e-03 CTHERM4 3 Ta 3.579e-02

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COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 $^\circ\text{C})$







COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 $^\circ\text{C})$





Recovery with LTspice[®] V_p parameter and simplified model of recovery tester



COMPARISON OF MODEL WITH MEASURED DATA (T_J = 125 $^\circ\text{C})$





Notes

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