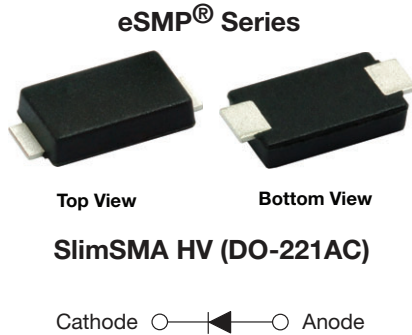


650 V Gen 3 Power SiC Merged PIN Schottky Diode, 2 A



LINKS TO ADDITIONAL RESOURCES



FEATURES

- Minimum creepage distance 3.2 mm guaranteed by design
- Comparative Tracking Index: CTI ≥ 600
- High CTI molding compound provides excellent electrical insulation at relevant working voltages
- Positive V_F temperature coefficient for easy paralleling
- Virtually no recovery tail and no switching losses
- Temperature invariant switching behavior
- 175 °C maximum operating junction temperature
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- MPS structure for high ruggedness to forward current surge events
- Meets JESD 201 class 2 whisker test
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

DESCRIPTION / APPLICATIONS

Wide band gap SiC based 650 V Schottky diode, designed for high performance and ruggedness.

Optimized for extreme high-speed hard switching over a wide temperature range. It is suited for demanding applications, such as bootstrap and anti-parallel diodes in AC/DC and DC/DC converters.

MECHANICAL DATA

Case: SlimSMA HV (DO-221AC)

Molding compound meets UL 94 V-0 flammability rating
Base P/N-M3 - halogen-free, RoHS-compliant

Terminals: matte tin plated leads, solderable per J-STD-002

PRIMARY CHARACTERISTICS	
$I_F^{(2)}$	2 A
V_R	650 V
V_F at I_F at 25 °C, typ.	1.30 V
T_J max.	175 °C
I_R at V_R at 175 °C	2.0 μ A
Q_C ($V_R = 400$ V)	7.2 nC
Package	SlimSMA HV (DO-221AC)
Circuit configuration	Single

MAXIMUM RATINGS ($T_A = 25$ °C unless otherwise specified)				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage	V_{RRM}		650	V
Continuous forward current	I_F	$T_M = 140$ °C (DC) ⁽¹⁾	2	A
DC blocking voltage	V_{DC}		650	V
Repetitive peak forward current	I_{FRM}	$T_M = 25$ °C, $f = 50$ Hz, square wave, DC = 25 %	8	A
Non-repetitive peak forward surge current	I_{FSM}	$T_M = 25$ °C, $t_p = 10$ ms, half sine wave	16.5	
		$T_M = 110$ °C, $t_p = 10$ ms, half sine wave	14	
Power dissipation	$P_{tot}^{(1)}$	$T_M = 25$ °C	12.5	W
		$T_M = 110$ °C	5.4	
	$P_{tot}^{(2)}$	$T_M = 25$ °C	9.7	W
		$T_M = 110$ °C	4.2	
i^2t value	$\int i^2 dt$	$T_M = 25$ °C	1.4	A ² s
		$T_M = 110$ °C	1.0	
Operating junction and storage temperatures	$T_J^{(3)}, T_{Stg}$		-55 to +175	°C

Notes

(1) Based on typical R_{th}

(2) Based on maximum R_{th}

(3) The heat generated must be less than the thermal conductivity from junction-to-ambient: $dP_D/dT_J < 1/R_{\theta JA}$

ELECTRICAL SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward voltage	V_F	$I_F = 2\text{ A}$	-	1.30	1.50	V
		$I_F = 2\text{ A}, T_J = 150\text{ }^\circ\text{C}$	-	1.45	1.70	
		$I_F = 2\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	1.50	-	
Reverse leakage current	I_R	$V_R = V_R\text{ rated}$	-	0.1	15	μA
		$V_R = V_R\text{ rated}, T_J = 150\text{ }^\circ\text{C}$	-	0.5	30	
		$V_R = V_R\text{ rated}, T_J = 175\text{ }^\circ\text{C}$	-	2.0	-	
Total capacitance	C	$V_R = 1\text{ V}, f = 1\text{ MHz}$	-	100	-	pF
		$V_R = 400\text{ V}, f = 1\text{ MHz}$	-	12.5	-	
Total capacitive charge	Q_C	$V_R = 400\text{ V}, f = 1\text{ MHz}$	-	7.2	-	nC

THERMAL - MECHANICAL SPECIFICATIONS ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Thermal resistance, junction to mount	$R_{thJM}^{(1)}$		-	12	15.5	$^\circ\text{C/W}$
Marking device				C207		

Note

(1) Thermal resistance junction-to-mount follows JEDEC® 51-14 transient dual interface test method (TDIM)

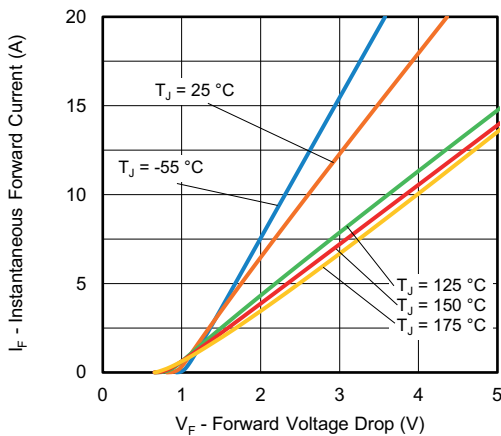


Fig. 1 - Typical Forward Voltage Drop Characteristics

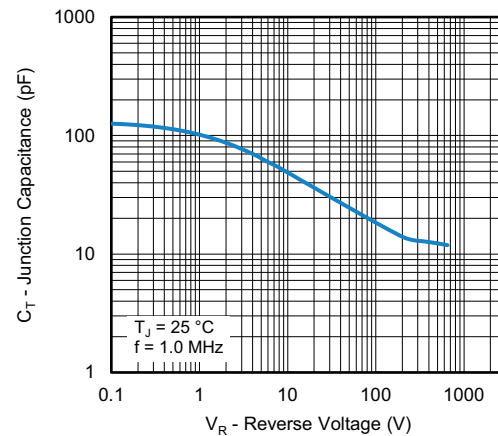


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

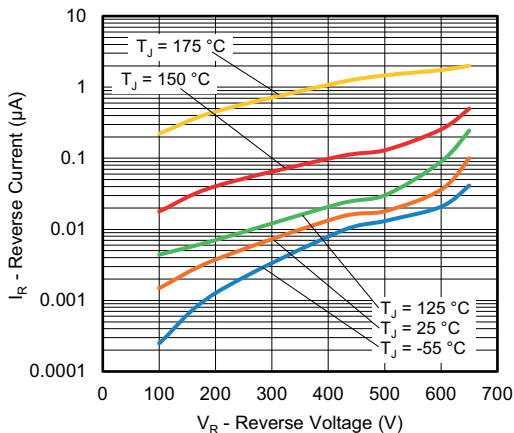


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

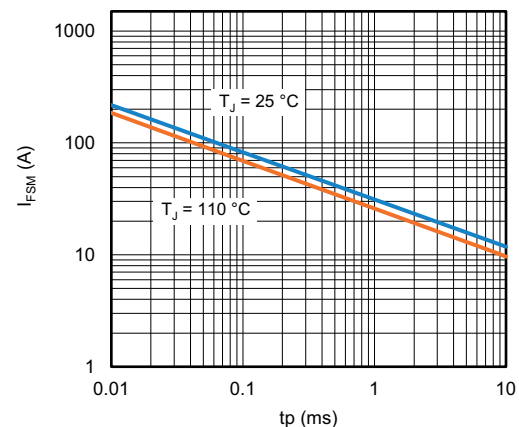


Fig. 4 - Non-Repetitive Peak Forward Surge Current vs. Pulse Duration (Square Wave)

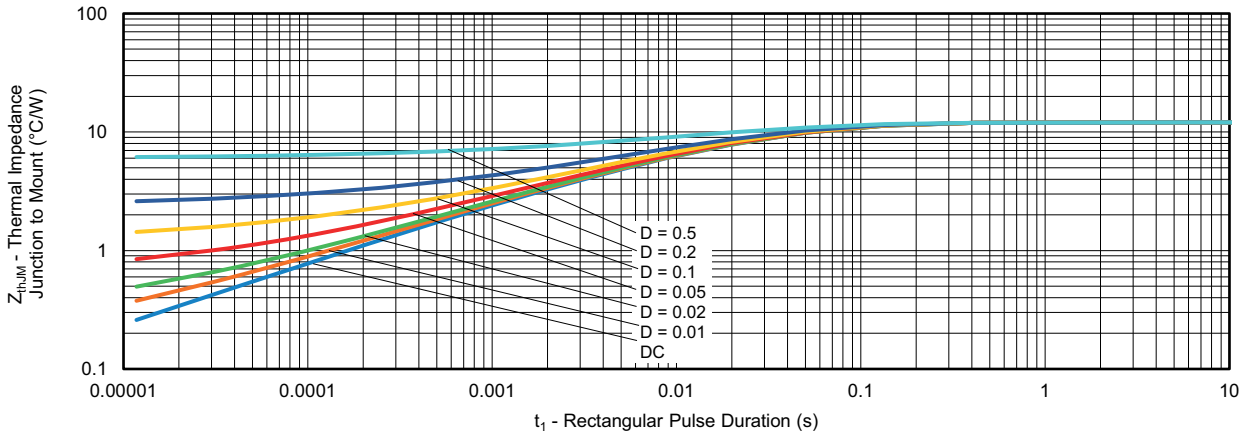


Fig. 5 - Typical Thermal Impedance Z_{thJM} Characteristics

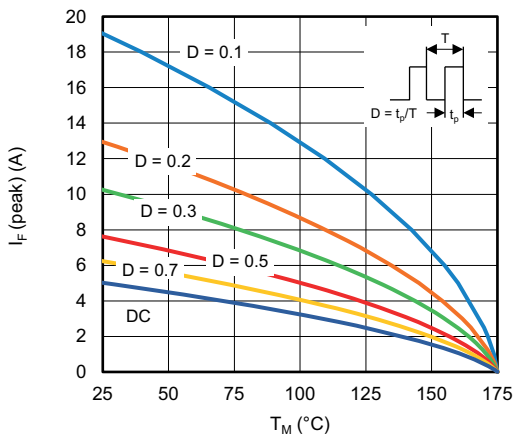


Fig. 6 - Peak Forward Current vs. Maximum Allowable Mount Temperature

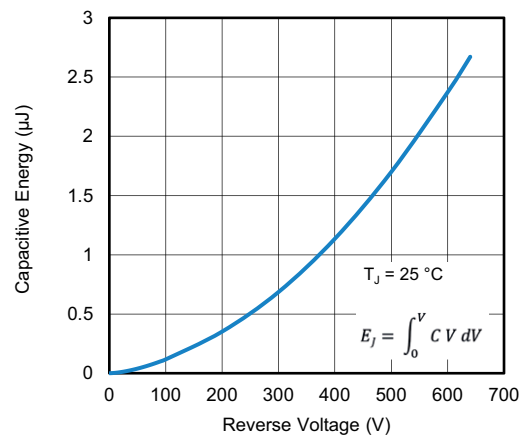


Fig. 8 - Typical Capacitive Energy vs. Reverse Voltage

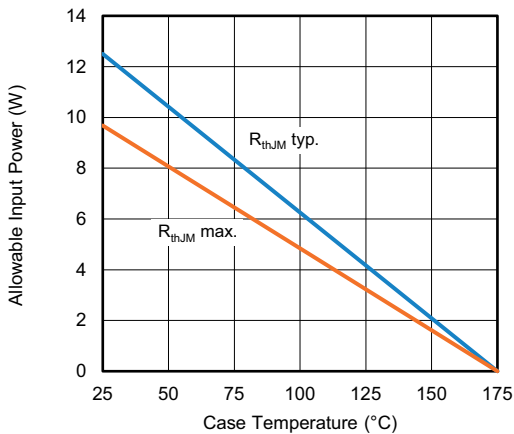


Fig. 7 - Forward Power Loss Characteristics

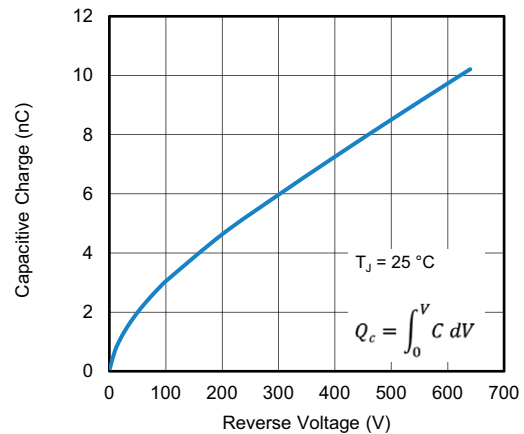
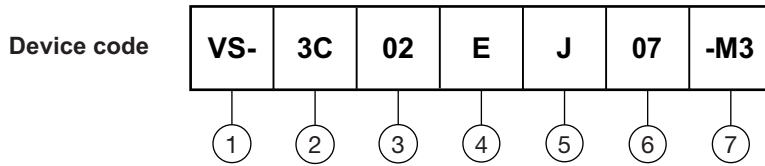


Fig. 9 - Typical Capacitive Charge vs. Reverse Voltage



ORDERING INFORMATION TABLE



- 1** - Vishay Semiconductors product
- 2** - 3C = SiC diode, generation 3
- 3** - Current rating (02 = 2 A)
- 4** - E = single diode
- 5** - J = SlimSMA HV package
- 6** - Voltage rating: (07 = 650 V)
- 7** - Environmental digit:
-M3 = halogen-free, RoHS-compliant, and termination lead (Pb)-free

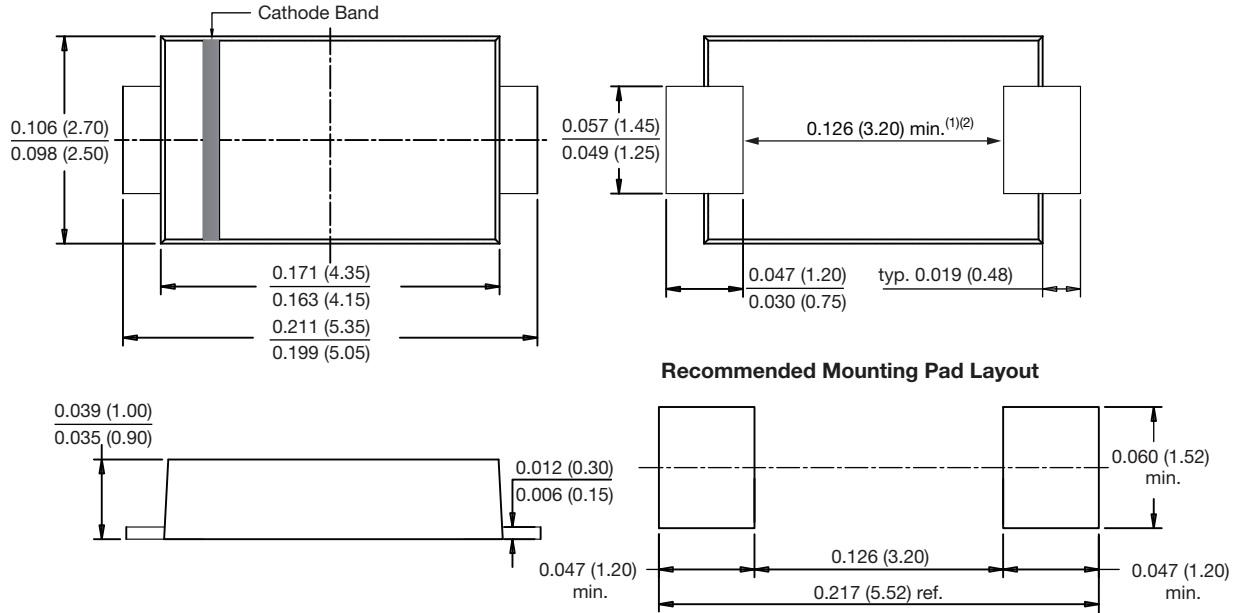
ORDERING INFORMATION			
PREFERRED P/N	UNIT WEIGHT (g)	BASE QUANTITY	PACKAGING DESCRIPTION
VS-3C02EJ07-M3/H	0.032	3500 per reel	7" diameter plastic tape and reel
VS-3C02EJ07-M3/I	0.032	14 000 per reel	13" diameter plastic tape and reel

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?97278
Part marking information	www.vishay.com/doc?98699
Packaging information	www.vishay.com/doc?98714



SlimSMA HV (DO-221AC)

DIMENSIONS in inches (millimeters)



Notes

- (1) Minimum creepage distance is defined and guaranteed by design
- (2) For high voltage applications, end users should consider the relevant guidelines and normative on creepage and clearance distances between device terminals and PCB pads.



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