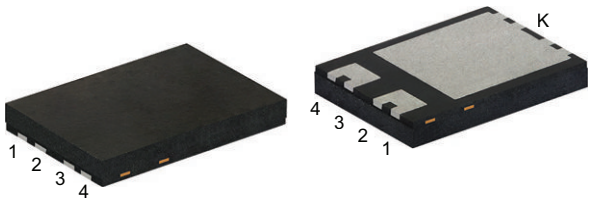
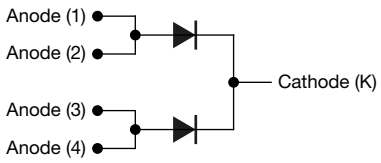
Ultrafast Rectifier, 2 x 7.5 A FRED Pt®



DFN6546A



FEATURES

- Very low profile - typical height of 0.88 mm
- Ideal for automated placement
- Wettable flanks allows easy inspection with AOI (automated optical inspection). No X-ray necessary
- Low forward voltage drop, low power losses
- Low leakage current
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- AEC-Q101 qualified
- For PFC, CRM snubber operation
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

RoHS COMPLIANT

HALOGEN FREE

LINKS TO ADDITIONAL RESOURCES

Ultra Librarian EDA / CAD

PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	2 x 7.5 A
V_R	200 V
V_F at I_F	0.75 V
t_{rr} (typ.)	15 ns
I_{FSM}	124 A
T_J max.	175 °C
Package	DFN6546A
Circuit configuration	Common cathode

TYPICAL APPLICATIONS

For use in high frequency inverters, DC/DC converters, freewheeling diodes, clamping and snubber, polarity protection, and LED lighting

MECHANICAL DATA

Case: DFN6546A

Molding compound meets UL 94 V-0 flammability rating

Terminals: matte tin plated leads, solderable per J-STD-002, meets JESD 201 class 2 whisker test

Polarity: color band denotes cathode end

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Peak repetitive reverse voltage, per leg	V_{RRM}		200	V
Average rectified forward current, per leg	$I_{F(AV)}$	T_M = 152 °C, D = 0.50	7.5	A
Non-repetitive peak surge current, per leg	I_{FSM}	T_J = 25 °C, 10 ms sine pulse	124	
Operating junction and storage temperatures	T_J, T_{Stg}		-55 to +175	°C

ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise specified)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Breakdown voltage, blocking voltage, per leg	V_{BR}, V_R	I_R = 100 µA	200	-	-	V
Forward voltage, per leg	V_F	I_F = 7.5 A	-	0.9	1.1	
		I_F = 7.5 A, T_J = 150 °C	-	0.75	0.85	
Reverse leakage current, per leg	I_R	V_R = V_R rated	-	-	1	µA
		T_J = 150 °C, V_R = V_R rated	-	-	150	
Junction capacitance, per leg	C_T	V_R = 200 V	-	25	-	pF

DYNAMIC RECOVERY CHARACTERISTICS (T_J = 25 °C unless otherwise specified)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Reverse recovery time, per leg	t_{rr}	I_F = 0.5 A, I_R = 1 A, I_{rr} = 0.25 A		-	15	25	ns
		T_J = 25 °C	I_F = 7.5 A, dI_F/dt = 500 A/µs, V_R = 200 V	-	12	-	
		T_J = 125 °C		-	21	-	
Peak recovery current, per leg	I_{RRM}	T_J = 25 °C		-	3.9	-	A
		T_J = 125 °C		-	7.2	-	
Reverse recovery charge, per leg	Q_{rr}	T_J = 25 °C		-	25	-	nC
		T_J = 125 °C		-	77	-	

THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Maximum junction and storage temperature range	T_J, T_{Stg}		-55	-	175	°C
Thermal resistance, junction to mount, per leg	R_{thJM} (1)		-	-	3.4	°C/W
Weight			-	0.086	-	9
Marking device		Case style DFN6546A	15CH2			

Note

(1) Thermal resistance junction to mount follows JEDEC® 51-14 transient dual interface test method (TDIM)

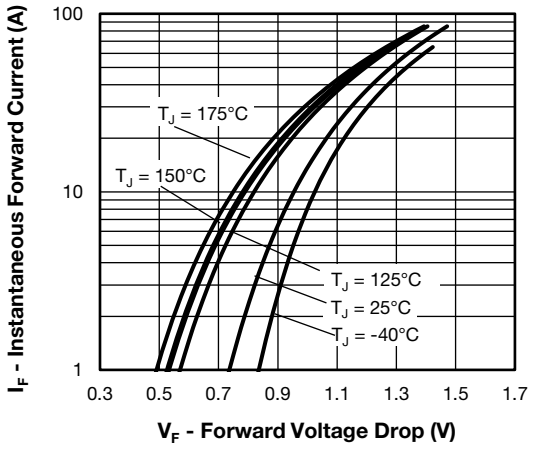


Fig. 1 - Typical Forward Voltage Drop Characteristics, per Leg

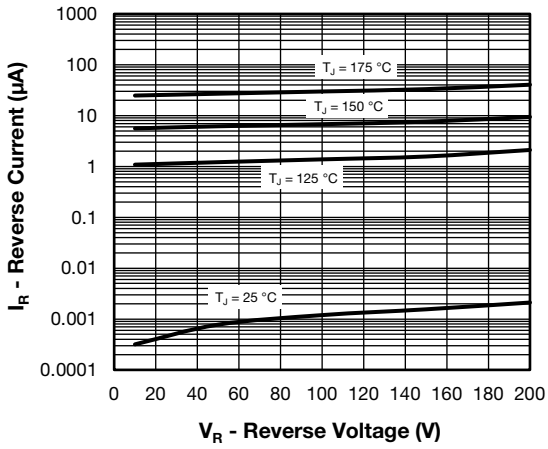


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage, per Leg

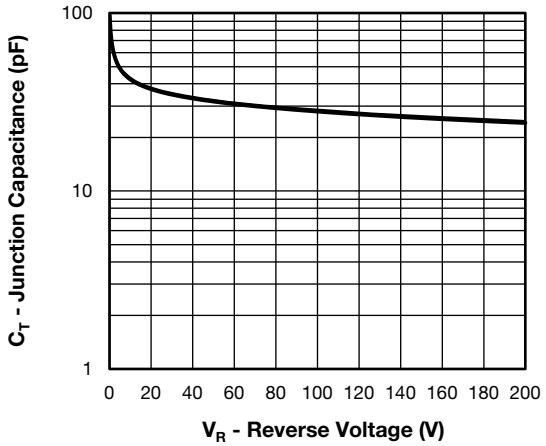


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage, per Leg

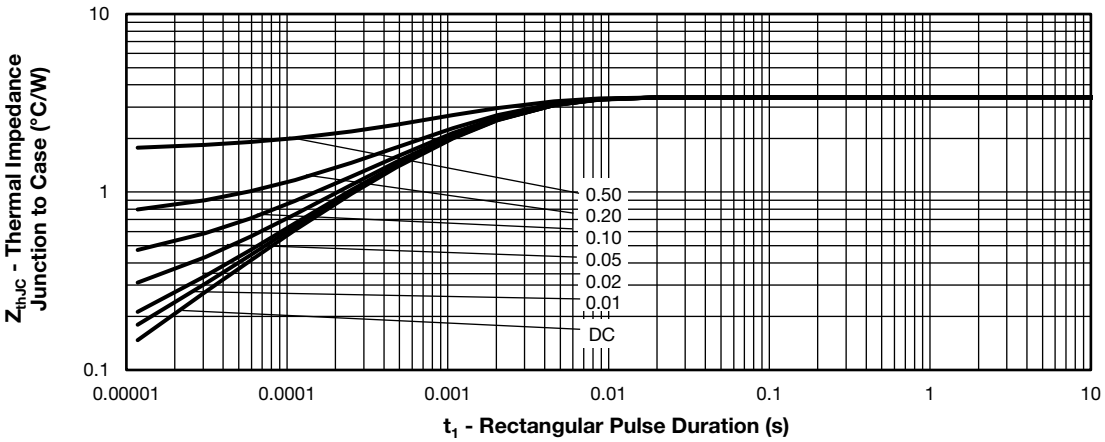


Fig. 4 - Maximum Transient Thermal Impedance, Junction to Mount, per Leg

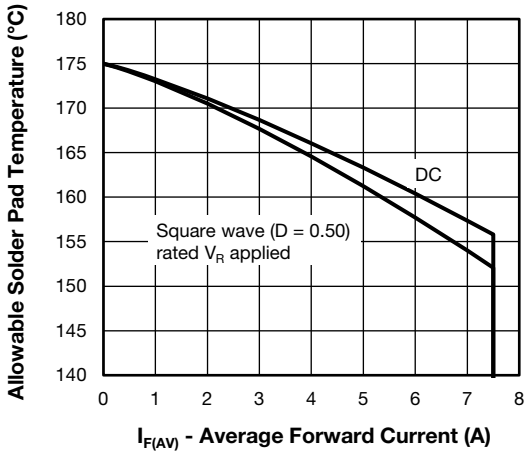


Fig. 5 - Maximum Allowable Mount Temperature vs. Average Forward Current, per Leg

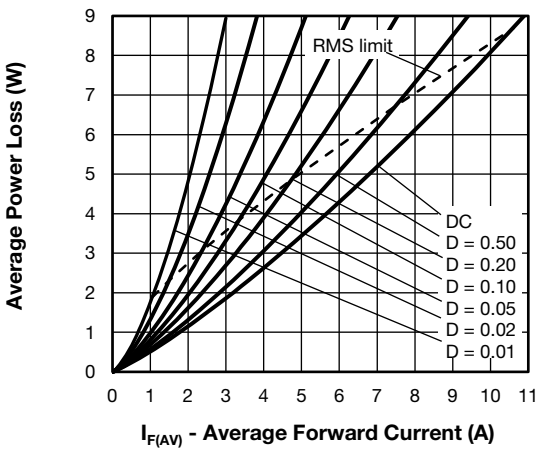


Fig. 6 - Forward Power Loss Characteristics, per Leg

Note

Formula used: $T_M = T_J - (Pd + Pd_{REV}) \times R_{thJM}$;
Pd = forward power loss = $I_{F(AV)} \times V_{FM}$ at ($I_{F(AV)}$/D) (see fig. 5);
Pd_{REV} = inverse power loss = $V_{R1} \times I_R$ (1 - D); I_R at V_{R1} = rated V_R

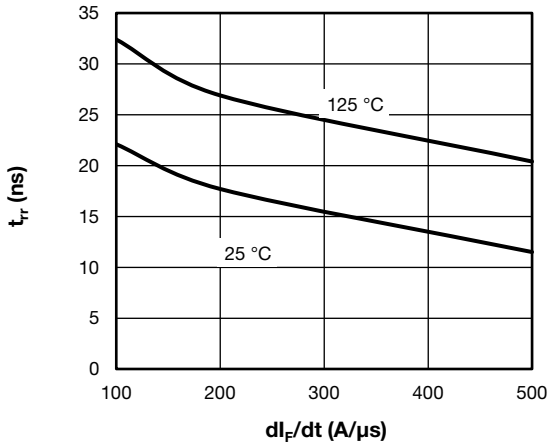


Fig. 7 - Typical Reverse Recovery Time vs. dI_F/dt, per Leg

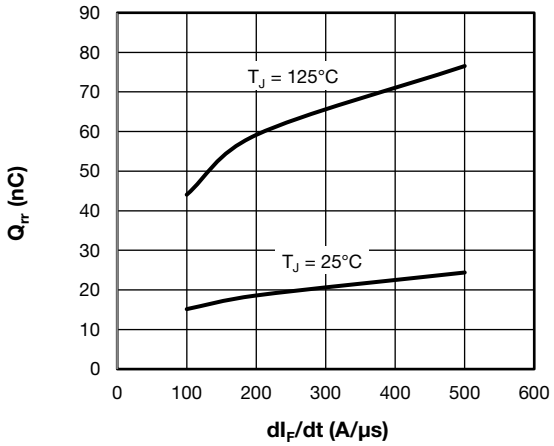


Fig. 8 - Typical Stored Charge vs. dI_F/dt, per Leg

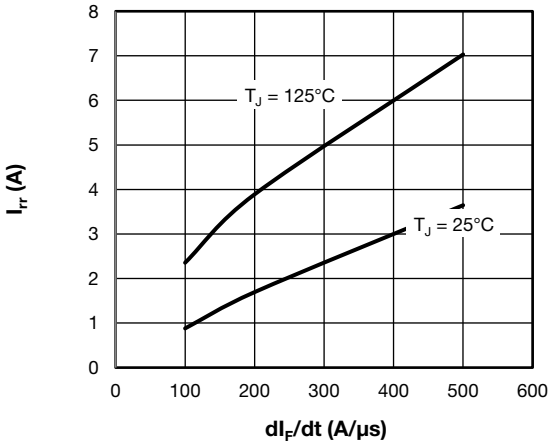
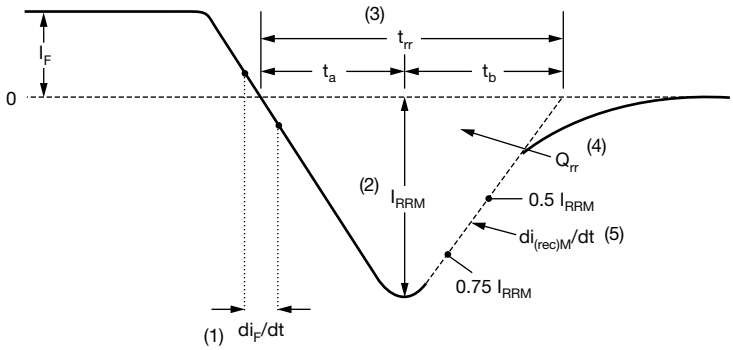


Fig. 9 - I_{rr} vs. dI/dt, per Leg



(1) di_F/dt - rate of change of current through zero crossing

(2) I_{RRM} - peak reverse recovery current

(3) t_{rr} - reverse recovery time measured from zero crossing point of negative going I_F to point where a line passing through 0.75 I_{RRM} and 0.50 I_{RRM} extrapolated to zero current.

(4) Q_{rr} - area under curve defined by t_{rr} and I_{RRM}

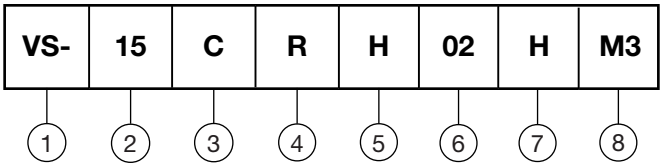
$$Q_{rr} = \frac{t_{rr} \times I_{RRM}}{2}$$

(5) $di_{(rec)M}/dt$ - peak rate of change of current during t_b portion of t_{rr}

Fig. 10 - Reverse Recovery Waveform and Definitions

ORDERING INFORMATION TABLE

Device code



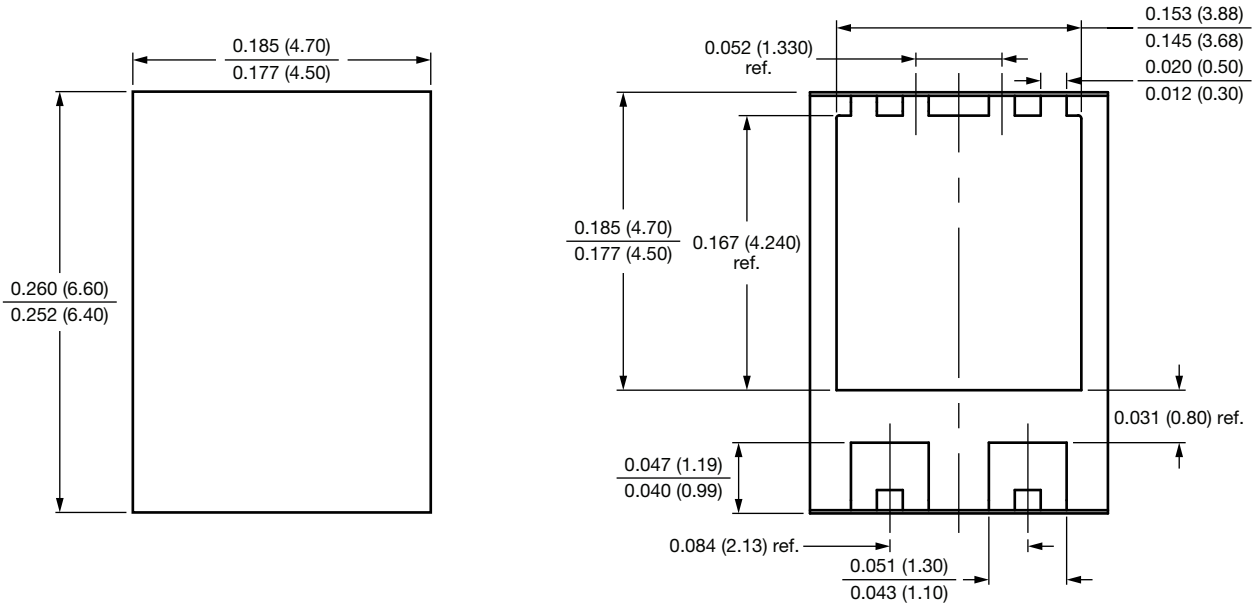
1 - Vishay Semiconductors product
2 - Current rating (15 = 15 A)
3 - Circuit configuration:
C = common cathode
4 - R = DFN6546A package
5 - Process type,
H = ultrafast recovery
6 - Voltage code (02 = 200 V)
7 - H = AEC-Q101 qualified
8 - M3 = halogen-free, RoHS-compliant, and terminations lead (Pb)-free

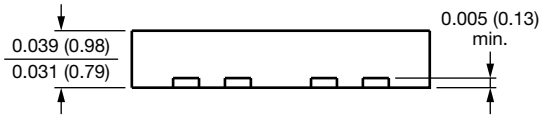
ORDERING INFORMATION (Example)			
PREFERRED P/N	**PREFERRED PACKAGE CODE**	**BASE QUANTITY**	**PACKAGING DESCRIPTION**
VS-15CRH02HM3/I	I	6000	13" diameter plastic tape and reel

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?97347
Part marking information	www.vishay.com/doc?97348
Packaging information	www.vishay.com/doc?98691

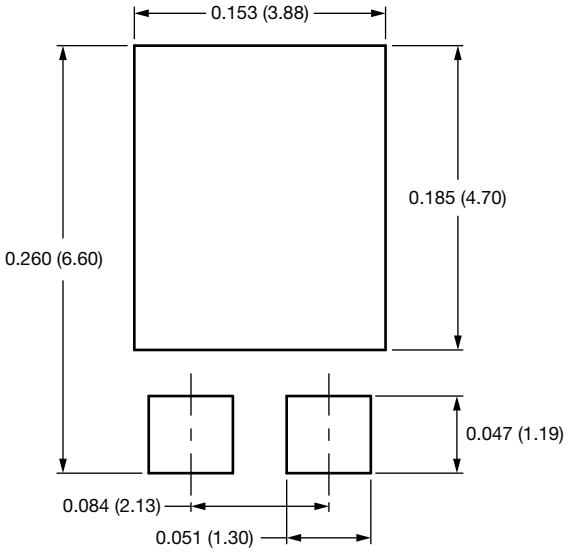
DFN6456, FRED Pt®

DIMENSIONS in inches (millimeters)





Mounting Pad Layout



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