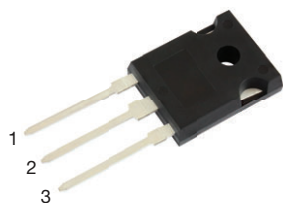
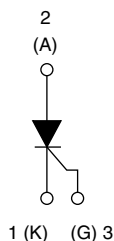


Thyristor High Voltage, Phase Control SCR, 50 A



TO-247AD 3L



FEATURES

- Designed and qualified according to JEDEC-JESD 47
- Flexible solution for reliable AC power rectification
- Easy control of peak current at charger power up to reduce passive / electromechanical components
- High dv/dt capability for improved immunity against fast voltage transients
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Battery chargers
- Renewable energy inverters
- High power semi-controlled and multi-phase bridges
- Pre-charge circuits bypass

DESCRIPTION

The VS-50TPS16 high voltage series of silicon controlled rectifiers are specifically designed for medium power switching, and phase control applications.

PRIMARY CHARACTERISTICS

$I_{T(AV)}$	50 A
V_{DRM}/V_{RRM}	1600 V
V_{TM} (typ.)	1.18 V
I_{GT} (typ.)	45 mA
T_J max.	125 °C
Package	TO-247AD 3L
Circuit configuration	Single SCR

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage	V_{RRM} / V_{DRM}		1600	V
On-state voltage	V_T	50 A, $T_J = 125\text{ °C}$	1.18	
Average rectified forward current	$I_{T(AV)}$		50	A
Maximum continuous RMS on-state current	I_{RMS}		79	
Non-repetitive peak surge current	I_{TSM}		700	
Maximum rate of rise	dV/dt		2000	V/μs
Operating junction and storage temperature range	T_J, T_{Stg}		-40 to +125	°C

VOLTAGE RATINGS

PART NUMBER	V_{RRM} / V_{DRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM} / I_{DRM} AT 125 °C mA
VS-50TPS16L-M3	1600	1700	10



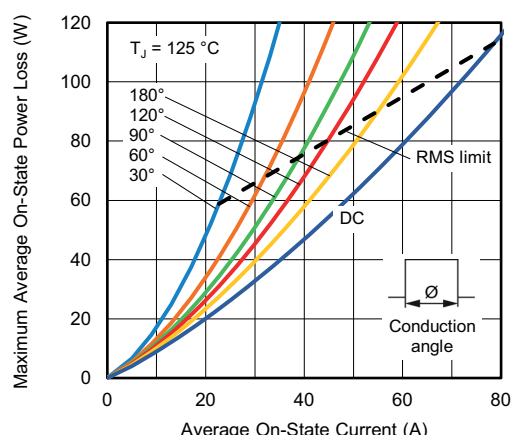
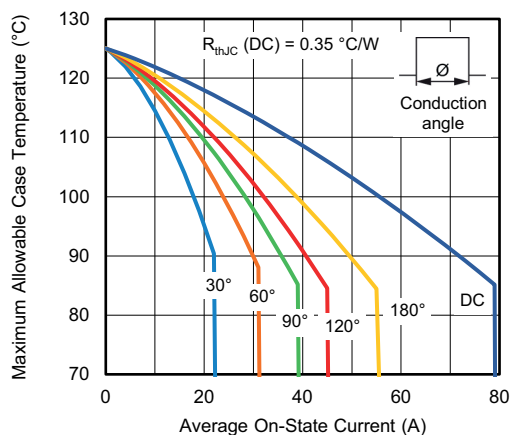
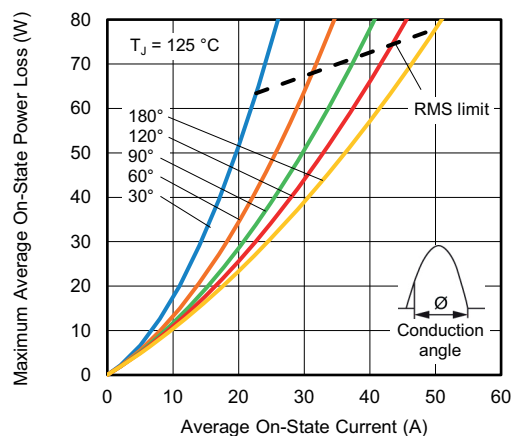
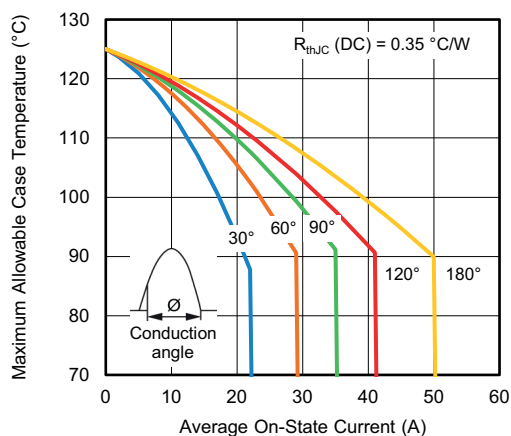
ABSOLUTE MAXIMUM RATINGS						
PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Maximum average on-state current	$I_{T(AV)}$	$T_C = 90\text{ }^{\circ}\text{C}$, 180° conduction half sine wave		-	50	A
Maximum continuous RMS on-state current as AC switch	$I_{T(RMS)}$			-	79	
Peak, one-cycle non-repetitive surge current	I_{TSM}	10 ms sine pulse, rated V_{RRM} applied	Initial $T_J = T_J$ maximum	-	590	
		10 ms sine pulse, no voltage reapplied		-	700	
I^2t for fusing	I^2t	10 ms sine pulse, rated V_{RRM} applied		-	1740	A ² s
		10 ms sine pulse, no voltage reapplied		-	2450	
$I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	$t = 0.1\text{ ms to }10\text{ ms}$, no voltage reapplied, $T_J = 125\text{ }^{\circ}\text{C}$		-	24500	A ² √s
Low level value of threshold voltage	$V_{T(TO)1}$	$T_J = 125\text{ }^{\circ}\text{C}$		-	0.81	V
High level value of threshold voltage	$V_{T(TO)2}$			-	0.94	
Low level value of on-state slope resistance	r_{t1}			-	8.75	mΩ
High level value of on-state slope resistance	r_{t2}			-	6.22	
On-state voltage	V_T	50 A, $T_J = 25\text{ }^{\circ}\text{C}$		1.22	1.3	V
		100 A, $T_J = 25\text{ }^{\circ}\text{C}$		1.45	1.6	
Rate of rise of turned-on current	di/dt	$T_J = 25\text{ }^{\circ}\text{C}$		-	150	A/μs
Holding current	I_H	Anode supply = 6 V, resistive load, $T_J = 25\text{ }^{\circ}\text{C}$		-	200	mA
Latching current	I_L			-	300	
Reverse and direct leakage current	I_{RRM}/I_{DRM}	$T_J = 25\text{ }^{\circ}\text{C}$		-	0.05	
		$T_J = 125\text{ }^{\circ}\text{C}$		-	10	
Rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 67 % V_{DRM} , Gate = open		-	2000	V/μs

TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Peak gate power	P _{GM}	10 ms sine pulse, no voltage reapplied		-	10	W
Average gate power	P _{G(AV)}			-	2.5	
Peak gate current	I _{GM}			-	2.5	A
Peak negative gate voltage	-V _{GM}			-	10	V
Required DC gate voltage to trigger	V _{GT}	T _J = -40 °C	Anode supply = 6 V resistive load	-	1.6	
		T _J = 25 °C		-	1.3	
		T _J = 125 °C		-	1.1	
Required DC gate to trigger	I _{GT}	T _J = -40 °C	Anode supply = 6 V resistive load	-	140	mA
		T _J = 25 °C		45	80	
		T _J = 125 °C		-	50	
DC gate voltage not to trigger	V _{GD}	T _J = 125 °C, V _{DRM} = rated value		-	0.2	V
DC gate current not to trigger	I _{GD}			-	3	mA

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS	TYP.	MAX.	UNITS
Turn-on time	t_{gt}	$I_T = 50\text{ A}$, $V_D = 50\text{ \% } V_{DRM}$, $I_{gt} = 300\text{ mA}$, $T_J = 25\text{ }^{\circ}\text{C}$	1.5	-	μs
Turn-off time	t_q	$I_T = 3\text{ A}$, $V_D = 55\text{ \% } V_{DRM}$, $dV/dt = 200\text{ V}/\mu\text{s}$, $I_{gt} = 500\text{ mA}$, $di/dt = 10\text{ A}/\mu\text{s}$, $V_R = 50\text{ V}$, $T_J = 25\text{ }^{\circ}\text{C}$	60	-	



THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS	TYP.	MAX.	UNITS
Maximum junction and storage temperature range	T _J , T _{Stg}		-40	125	°C
Maximum thermal resistance, junction to case	R _{thJC}		-	0.35	°C/W
Maximum thermal resistance, junction to ambient	R _{thJA}		-	40	
Typical thermal resistance, case to heatsink	R _{thCS}	Mounting surface, smooth, and greased	0.2	-	
Approximate weight			6		g
			0.21		oz.
Mounting torque	minimum		6 (5)		kgf · cm (lbf · in)
	maximum		12 (10)		
Marking device		Case style Super TO-247AD 3L	50TPS16L		



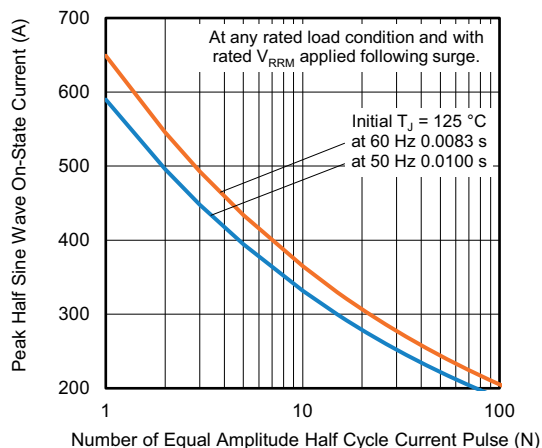


Fig. 5 - Maximum Non-Repetitive Surge Current

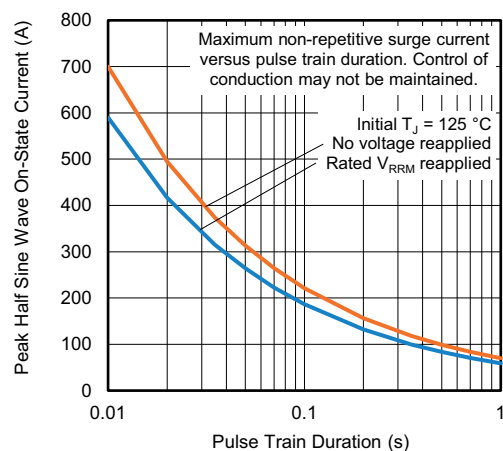


Fig. 6 - Maximum Non-Repetitive Surge Current

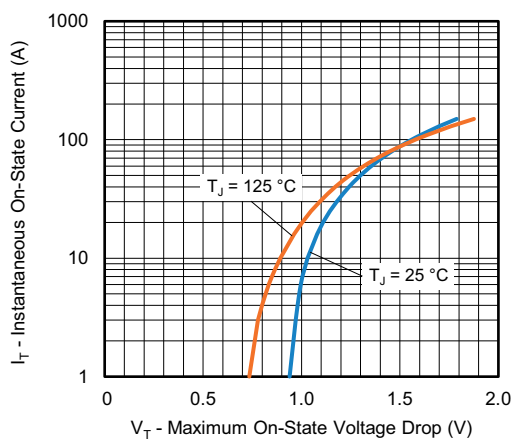


Fig. 7 - On-State Voltage Drop Characteristics

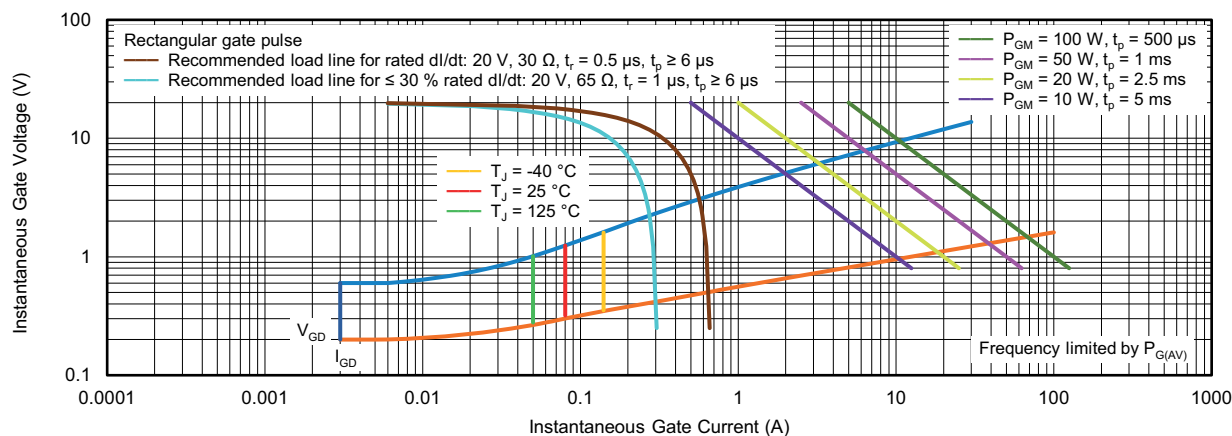


Fig. 8 - Gate Characteristics

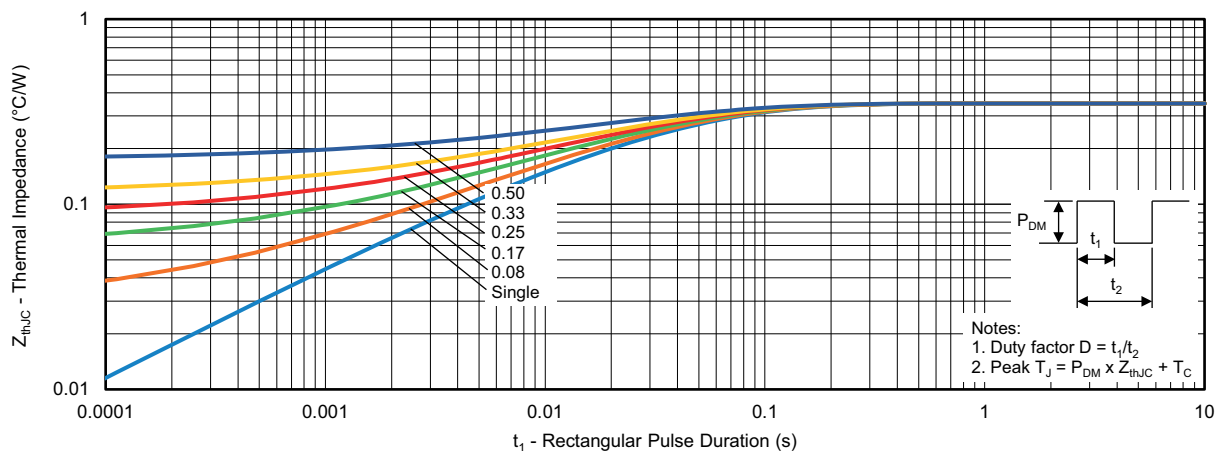


Fig. 9 - Thermal Impedance Z_{thJC} Characteristics

ORDERING INFORMATION TABLE

Device code	VS-	50	T	P	S	16	L	-M3
	①	②	③	④	⑤	⑥	⑦	⑧

- 1** - Vishay Semiconductors product
- 2** - Current code (50 = 50 A)
- 3** - Circuit configuration:
T = thyristor
- 4** - P = TO-247AD package
- 5** - Type of silicon:
S = standard recovery rectifier
- 6** - Voltage code (16 = 1600 V)
- 7** - Package L = long lead
- 8** - -M3 = halogen-free, RoHS-compliant, and terminations lead (Pb)-free

ORDERING INFORMATION (example)			
PREFERRED P/N	QUANTITY PER TUBE	MINIMUM ORDER QUANTITY	PACKAGING DESCRIPTION
VS-50TPS16L-M3	25	contact factory	Antistatic plastic tubes

LINKS TO RELATED DOCUMENTS		
Dimensions	TO-247AD 3L	www.vishay.com/doc?95626
Part marking information	TO-247AD 3L	www.vishay.com/doc?95007



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