Vishay General Semiconductor

Surface-Mount Glass Passivated Rectifier



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SMB (DO-214AA)

Cathode O Anode

LINKS TO ADDITIONAL RESOURCES



PRIMARY CHARACTERISTICS					
I _{F(AV)}	2.0 A				
V _{RRM}	400 V, 600 V, 800 V, 1000 V				
I _{FSM}	70 A				
I _R	1.0 µA				
V_F at I_F = 2.0 A	0.86 V				
T _J max.	150 °C				
Package	SMB (DO-214AA)				
Circuit configuration	Single				

FEATURES

- Low profile package
- Ideal for automated placement
- Glass passivated chip junction
- Low forward voltage drop
- Low leakage current
- · High forward surge capability
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

TYPICAL APPLICATIONS

For use in general purpose rectification of power supplies, inverters, converters and freewheeling diodes for consumer, medical and telecommunication.

MECHANICAL DATA

Case: SMB (DO-214AA)

Molding compound meets UL 94 V-0 flammability rating Base P/N-E3 - RoHS compliant, commercial grade Base P/N-M3 - halogen-free, RoHS compliant, and commercial grade

Terminals: matte tin plated leads, solderable per J-STD-002 and JESD 22-B102

E3 and M3 suffix meets JESD 201 class 1A whisker test

Polarity: color band denotes the cathode end

MAXIMUM RATINGS ($T_A = 25 \text{ °C}$ unless otherwise noted)							
PARAMETER	SYMBOL	S2BG	S2BJ	S2BK	S2BM	UNIT	
Device marking code		2G	2J	2K	2M		
Maximum repetitive peak reverse voltage	V _{RRM}	400	600	800	1000	V	
Maximum RMS voltage	V _{RMS}	280	420	560	700	V	
Maximum DC forward current (fig. 1)		2.0				А	
		1.3				А	
Peak forward surge current 8.3 ms single half sine-wave superimposed on rated load	I _{FSM}	70				А	
Operating and storage temperature range	T_J ⁽³⁾ , T_{STG}		-55 to	+150		°C	

Notes

(1) Mounted on 8 mm x 8 mm pad areas, 1 oz. FR4 PCB

⁽²⁾ Free air mounted on recommended copper pad area

 $^{(3)}$ The heat generated must be less than the thermal conductivity from junction-to-ambient: $dP_D/dT_J < 1/R_{\theta JA}$





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ELECTRICAL CHARACTERISTICS (T _A = 25 °C unless otherwise noted)							
PARAMETER	TEST CONDITIONS		SYMBOL	TYP.	MAX.	UNIT	
Instantaneous forward voltage	I _F = 1.0 A	T - 25 °C	- V _F ⁽¹⁾	0.90	-	v	
	I _F = 2.0 A	T _J = 25 °C		0.96	1.1		
	I _F = 1.0 A	T _{.1} = 125 °C		0.78	-		
	I _F = 2.0 A	13 = 125 C		0.86	1.05		
Reverse current	Rated V _B	T _J = 25 °C	- I _R ⁽²⁾	0.15	1.0	μA	
	naleu v _R	T _J = 125 °C		36	125		
Typical reverse recovery time	I _F = 0.5 A, I _R = I _{rr} = 0.25 A	$I_F = 0.5 \text{ A}, I_R = 1.0 \text{ A}, I_{rr} = 0.25 \text{ A}$		2.0		μs	
Typical junction capacitance	Rated V _B = 4.	Rated $V_{B} = 4.0 V, 1 MHz$		16		pF	

Notes

 $^{(1)}\,$ Pulse test: 300 μs pulse width, 1 % duty cycle

⁽²⁾ Pulse test: Pulse width, \leq 40 ms

THERMAL CHARACTERISTICS ($T_A = 25 \text{ °C}$ unless otherwise noted)							
PARAMETER	SYMBOL	S2BG	S2BJ	S2BK	S2BM	UNIT	
Typical thermal resistance	R _{0JA} ⁽¹⁾⁽²⁾	107				°C/W	
Typical thermal resistance	R _{0JM} ⁽³⁾	7.2				0/10	

Notes

⁽¹⁾ The heat generated must be less than the thermal conductivity from junction-to-ambient: $dP_D/dT_J < 1/R_{\theta,JA}$

⁽²⁾ Thermal resistance junction-to-ambient to follow JEDEC[®] 51-2A, device mounted on FR4 PCB, 2 oz. standard footprint

(3) Thermal resistance junction-to-mount to follow JEDEC® 51-14, transient dual interface test method (TDIM)

ORDERING INFORMATION (Example)							
PREFERRED P/N	UNIT WEIGHT (g)	PREFERRED PACKAGE CODE	BASE QUANTITY	DELIVERY MODE			
S2BJ-M3/I	0.096	I	3200	13" diameter plastic tape and reel			
S2BJ-E3/I	0.096	I	3200	13" diameter plastic tape and reel			

RATINGS AND CHARACTERISTICS CURVES (T_A = 25 °C unless otherwise noted)

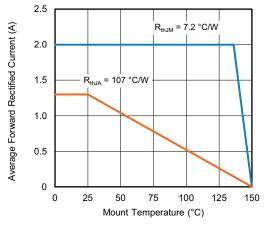


Fig. 1 - Maximum Forward Current Derating Curve

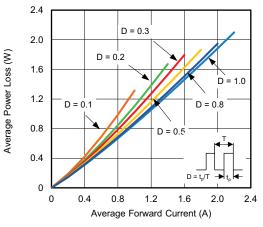


Fig. 2 - Forward Power Loss Characteristics

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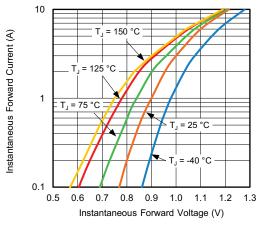


Fig. 3 - Typical Instantaneous Forward Characteristics

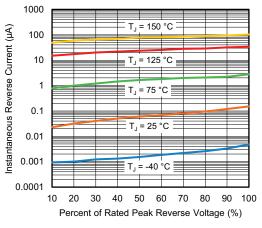
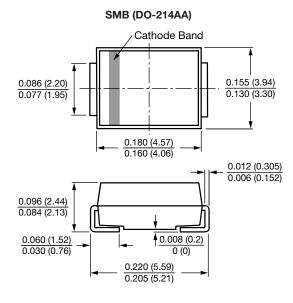


Fig. 4 - Typical Reverse Characteristics

PACKAGE OUTLINE DIMENSIONS in inches (millimeters)



S2BG, S2BJ, S2BK, S2BM

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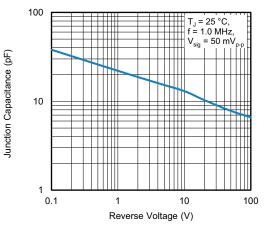


Fig. 5 - Typical Junction Capacitance

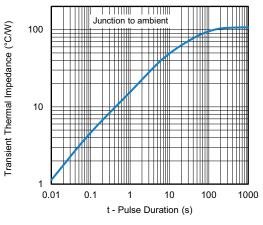
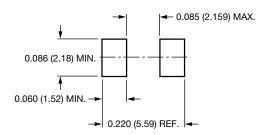


Fig. 6 - Typical Transient Thermal Impedance

Mounting Pad Layout



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