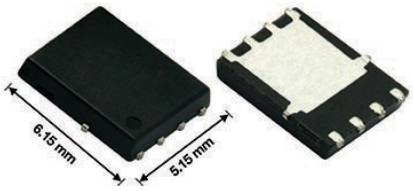
Standard-Level 40 V MOSFETs in the PowerPAK® SO-8 Single Package Prevent False Triggering and Reduce Noise in Motor Control Circuits, Provide High $V_{th(min)}$ > 2.5 V and Q_{gd} / Q_{gs} Ratios < 1

Product Benefits:

- Offered in the 6.15 mm by 5.15 mm PowerPAK® SO-8 single package
- High minimum gate-source threshold voltage > 2.5 V avoids false trigger signals
- Optimized Q_{gd} / Q_{gs} ratios < 1 reduce gate induced-voltage fluctuations
- Available with a range of typical on-resistance values from 0.9 mΩ to 2.5 mΩ at 10 V
- Provide gate charge values from 32.6 nC to 82 nC
- 100 % R_G- and UIS-tested
- RoHS-compliant, and halogen-free



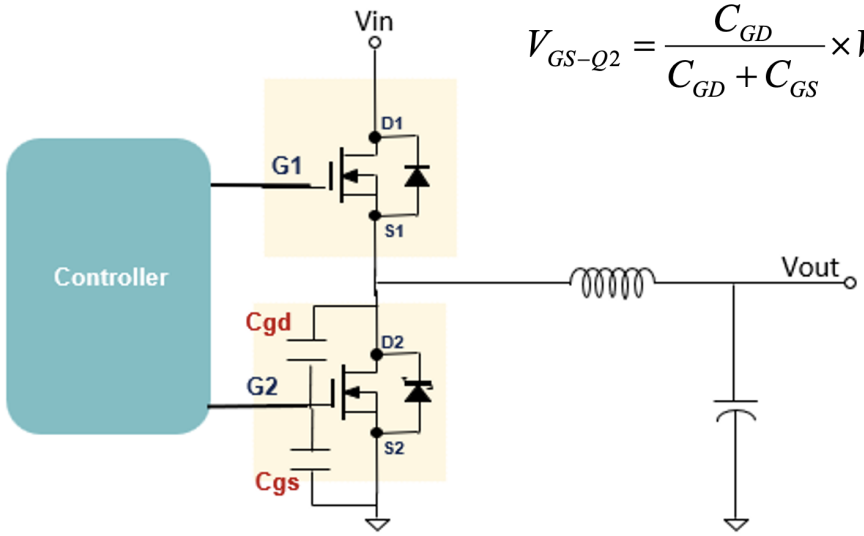
Market Applications:

- Half Bridge, Full Bridge, Synchronous rectification and DC/DC conversion in BLDC motors, power tools, drones, and automation systems

The News:

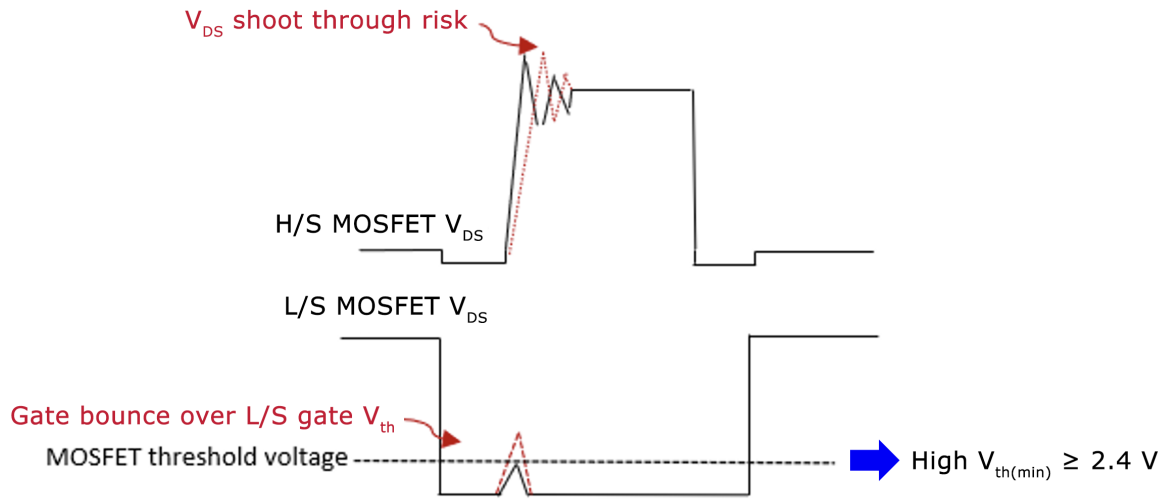
Vishay Intertechnology introduces four new 40 V TrenchFET® Gen IV standard-level n-channel power MOSFETs in the 6.15 mm by 5.15 mm PowerPAK SO-8 single package. Optimized for the noisy environments of motor control circuits, the Vishay Siliconix SIR5402DP, SIR5404DP, SIR5406DP, and SIR5408DP combine a high minimum gate-source threshold voltage of greater than 2.5 V with Q_{gd} / Q_{gs} ratios of less than 1.

- The devices' high minimum gate-source threshold voltage prevents false MOSFET triggering induced by the gate in motor control circuits
- The MOSFETs' optimized Q_{gd} / Q_{gs} ratios reduce gate-induced voltage fluctuations and the impact of gate noise



$$V_{GS-Q2} = \frac{C_{GD}}{C_{GD} + C_{GS}} \times V_{SW} < V_{GS(TH)-Q2} \Rightarrow \frac{Q_{GD}}{Q_{GS}} < 1$$

In a synchronous buck converter, the gate-source voltage of the low-side MOSFET (Q2) can rise due to capacitive coupling from drain voltage transients on the high side MOSFET (Q1). This induced V_{GS} is a function of the ratio $C_{GD}/(C_{GD} + C_{GS})$. To prevent unintentional turn-on of Q2 and potential shoot-through, the condition $V_{GS-Q2} < V_{GS(th)-Q2}$ must be satisfied. This is achieved when $Q_{GD}/Q_{GS} < 1$.



Shown are V_{DS} waveforms for high side (H/S) and low side (L/S) MOSFETs in a switching converter. During transitions, gate bounce over the L/S MOSFET's threshold voltage (V_{th}) can cause unintentional turn-on, leading to V_{DS} shoot-through in the H/S MOSFET. A high minimum threshold voltage ($V_{th(min)} \geq 2.4$ V) helps mitigate this risk.

The Key Specifications:

Part #		SIR5402DP	SIR5404DP	SIR5406DP	SIR5408DP
V_{DS}		40	40	40	40
V_{GS}		± 20	± 20	± 20	± 20
$R_{DS(on)}$	**@ 10 V (Typ.)**	0.9 mΩ	1.55 mΩ	1.9 mΩ	2.5 mΩ
	@ 10 V (Max.)	1.2 mΩ	1.85 mΩ	2.5 mΩ	3.2 mΩ
Q_g		82	61.5	44	32.6
Q_{gs}		26	20	14	10.5
Q_{gd}		18	14.5	10.5	7.5
Q_{gd} / Q_{gs} ratio		0.69	0.73	0.75	0.71
$V_{th(min)}$		2.5	2.5	2.5	2.5
Package		PowerPAK SO-8 single			

Availability:
Samples and production quantities of the new standard-level MOSFETs are available now, with a lead time of 13 weeks.

To access the product datasheets on the Vishay Website, go to
http://www.vishay.com/ppg?61684 (SIR5402DP)
http://www.vishay.com/ppg?61660 (SIR5404DP)
http://www.vishay.com/ppg?61690 (SIR5406DP)
http://www.vishay.com/ppg?61662 (SIR5408DP)

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