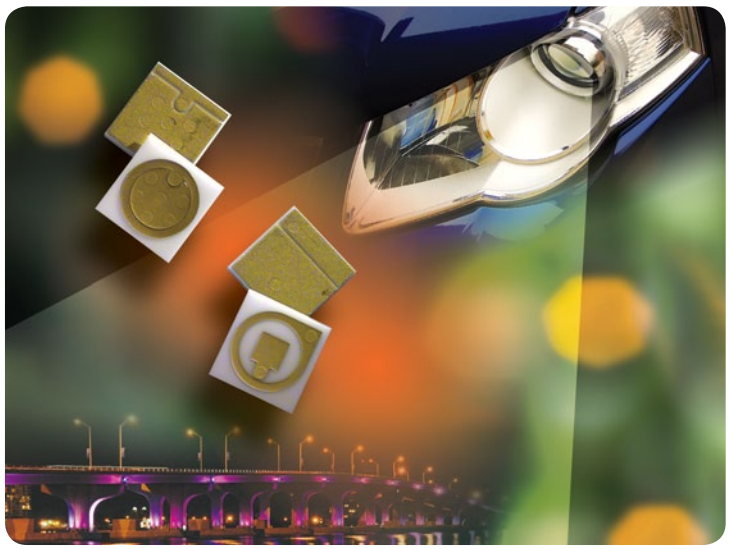
CERAMIC THIN FILM LED PACKAGE

Vishay Electro-Films

LED Submounts



INTRODUCTION

LED die performance is extremely sensitive to temperature. As junction temperature increases, LED efficiency drops. The lifetime of the LED is reduced and the overall flux of light emitted from the LED declines.

The typical efficiency of high-power LEDs is ~10 %. The remaining 90 % of the energy is dissipated as heat within the LED die. The rate by which this heat can be transferred away from the die determines the steady-state operating junction temperature and therefore determines the efficiency and reliability of the component.

DESIGN NOTES

The package can be custom designed to meet the needs of specific applications based on the design rules presented here and the general documents listed below. If your design is complete and you would like us to use your files, or if you would like us to help finalize your design, please contact us:

RESOURCES

- For technical questions contact efi@vishay.com
- HDI Design guidelines: www.vishay.com/doc?49387
- Integrated Microelectronic Interconnect Circuitry: www.vishay.com/doc?61082
- Sales Contacts: http://www.vishay.com/doc?99914

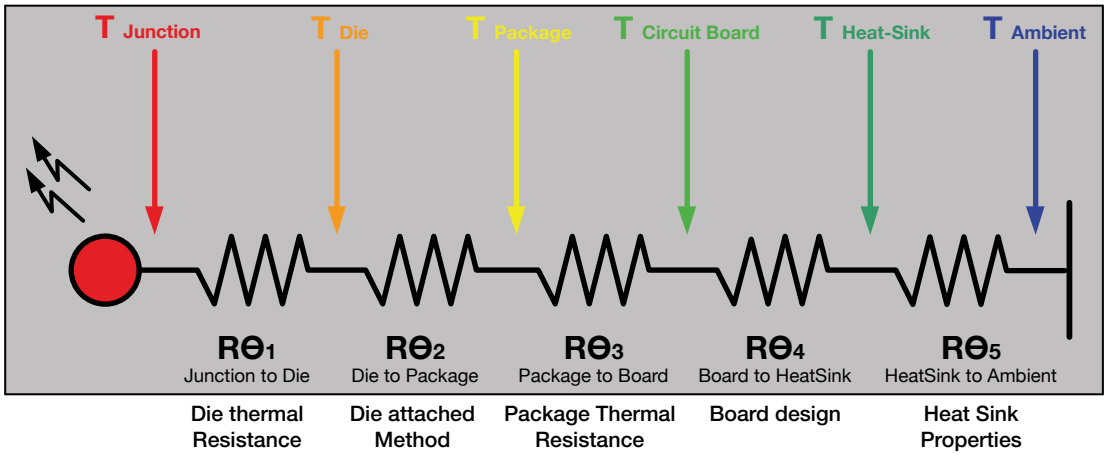
CERAMIC THIN FILM LED PACKAGE

Vishay Electro-Films

Thermal management is one of the biggest challenges facing LED-based light fixture designers. Vishay Electro-Films meets this challenge by utilizing its mature thermal-management solutions, which include the following capabilities:

- Thermally conductive Al_2O_3 or AlN substrate material as the LED package base
- Solid-filled copper vias to provide the shortest path through the substrate to carry and spread the heat away from the die
- Thick-patterned copper films to further enhance heat transfer towards the system heat sink
- Deposited Au/Sn eutectic solder to minimize thermal resistance between the die and package
- Second-level Au bumps to support eutectic/ultrasonic die attach of edge emitting diodes
- High quality aluminum reflective surfaces for increased reflectivity

The heat path in the light fixture can be modeled as a network of thermal resistors connected in series. The image below is a schematic representation of such a network:



The total thermal resistance between the junction and ambient is the sum of these five resistors. Minimizing the total thermal resistance is achieved by independently minimizing each of the five elements in the network. High-power LED packages are measured by their ability to facilitate low thermal resistance die attach techniques (minimizing RΘ2) and their ability to effectively carry the heat from the die to the next level of assembly (minimizing RΘ3).

Utilizing Vishay EFI's mature capabilities listed above allows designers to achieve both goals by facilitating high-temperature die attach (Au/Sn solder), shortening the transfer path (solid filled vias), and the use of low thermal resistance materials (thick copper patterns on ceramic substrates).

Vishay EFI has developed the LSUB as a standard ceramic submount for high-power LEDs. Samples of these parts are available upon request. Submounts can also be designed for specific applications.

Packages can be delivered in die form in waffle packs, or in wafer form to support automated assembly. Alumina substrates can be supplied with laser scoring for manual break after assembly.

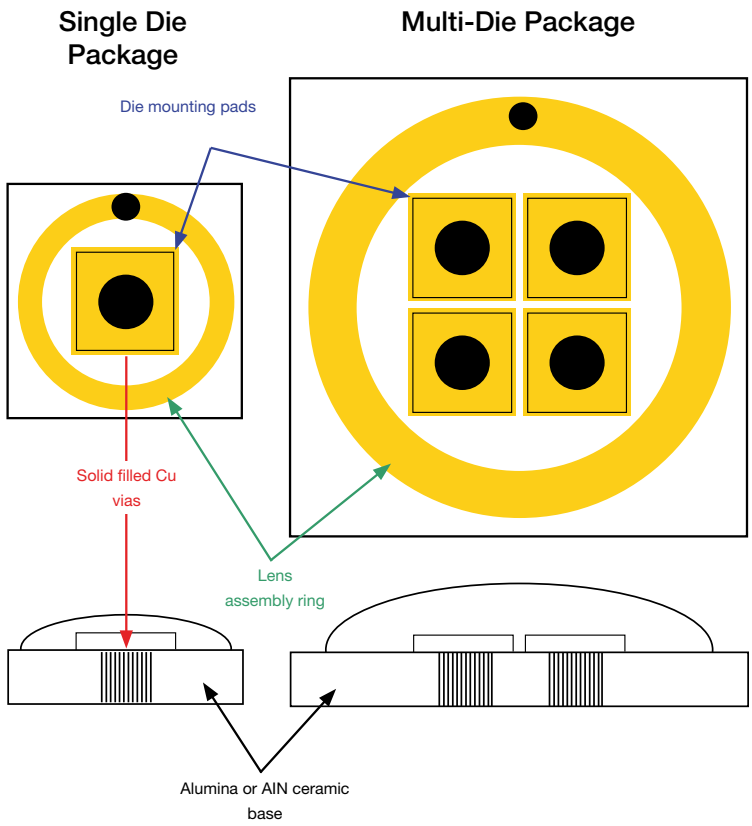
Typical Applications

- High brightness LED package
- Surface-mount LED package
- Packaging solutions for single chip and multi-chip packages
- General illumination, automotive lighting, and LCD backlighting

CERAMIC THIN FILM LED PACKAGE

Vishay Electro-Films

High-Brightness, High-Power LED Packages



Ceramic Material Selection					
Material	**Surface finish [µ" (µm)]**	**Standard thickness [mils (mm)]**	**Thermal conductivity @ 25 °C [W/mK]**	**CTE [ppm/°C]**	**Max substrate size [in (cm)]***
Alumina (96 %)	< 35 (0.89)	15 (0.381), 25 (0.635)	25	8.2	4.5 (11.43) x 4.5 (11.43)
Alumina (99.6 %)	< 4 (0.1)	15 (0.381), 25 (0.635)	35	8.4	4.5 (11.43) x 4.5 (11.43)
AIN	< 20 (0.5)	15 (0.381), 25 (0.635)	170	4.6	4.5 (11.43) x 4.5 (11.43)

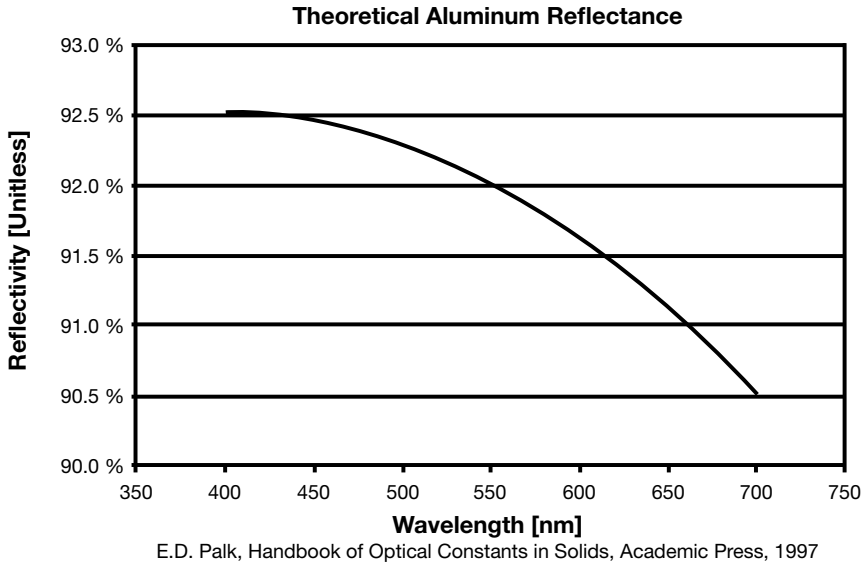
* Actual usable area is smaller than substrate size.

Standard Metallization				
Adhesion [Å]	**Conductor [µ" (µm)]**	**Barrier [µ" (µm)]**	**Interface [µ" (µm)]**	**Reflector [KÅ] (optional)**
Cr	Cu	Ni	Au	Al
750 ± 250	750 (19.05) min to 2000 (50.8) min	50 (1.27) min	50 (1.27) min	12 min

Aluminum surfaces allow high reflectivity throughout the visible spectrum.

CERAMIC THIN FILM LED PACKAGE

Vishay Electro-Films



E.D. Palk, Handbook of Optical Constants in Solids, Academic Press, 1997

Solid Filled Vias					
Substrate thickness [mil (mm)]	**Cu filled via thermal conductivity**	**Via diameter [mil (mm)]**	**Via center to center**	**Via edge to circuit edge**	**Via edge to pad edge [mil (mm)]**
15 (0.381)	375 W/mK	8 (0.203) to 23 (0.584)	2 x via diameter	1.5 x via diameter	3 (0.075)
25 (0.635)	375 W/mK	13 (0.330) to 38 (0.965)	2 x via diameter	1.5 x via diameter	3 (0.075)

Vishay EFI's unique via filling technology enables the use of bulk copper with typical thermal conductivity greater than 375 W/mK.

Deposited 80/20 Au/Sn			
Solder	**Thickness [µm]**	**Reflow temp [°C]**	**Solder bleed**
80/20 Au/Sn	2 to 8 ± 1	280 to 285	None

Layout Guidelines