

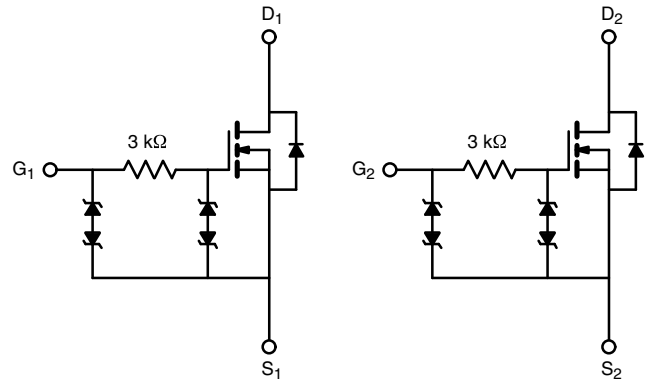
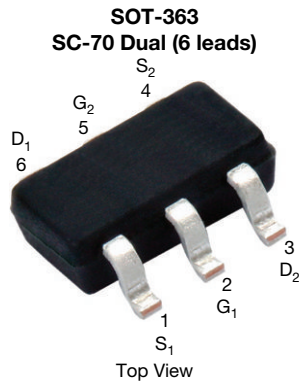
## Automotive Dual N-Channel 20 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	20
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.280
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 2.5$ V	0.360
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 1.8$ V	0.450
$I_D$ (A)	0.8
Configuration	Dual

### FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 %  $R_g$  tested
- Typical ESD protection: 800 V
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

 AUTOMOTIVE  
GRADE

**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

**Marking Code:** 8R

ORDERING INFORMATION	
Package	SC-70
Lead (Pb)-free and Halogen-free	SQ1912AEEH-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	20	V	
Gate-Source Voltage	$V_{GS}$	$\pm 12$		
Continuous Drain Current <sup>a</sup>	$I_D$	$T_C = 25$ °C	0.8	A
		$T_C = 125$ °C	0.8	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	0.8		
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	3		
Maximum Power Dissipation <sup>b</sup>	$P_D$	$T_C = 25$ °C	1.5	W
		$T_C = 125$ °C	0.5	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	$R_{thJA}$	220	°C/W	
Junction-to-Foot (Drain)	$R_{thJF}$	100		

### Notes

- Package limited.
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR4 material).



SPECIFICATIONS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		20	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		0.45	0.6	1.5	
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$		-	-	$\pm 1$	$\mu\text{A}$
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$		-	-	$\pm 10$	mA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	150	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{GS} = 4.5\text{ V}$	$V_{DS} \geq 5\text{ V}$	1.5	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}$	$I_D = 1.2\text{ A}$	-	0.200	0.280	$\Omega$
		$V_{GS} = 4.5\text{ V}$	$I_D = 1.2\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.423	
		$V_{GS} = 4.5\text{ V}$	$I_D = 1.2\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.510	
		$V_{GS} = 2.5\text{ V}$	$I_D = 1\text{ A}$	-	0.261	0.360	
		$V_{GS} = 1.8\text{ V}$	$I_D = 0.2\text{ A}$	-	0.320	0.450	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 1.2\text{ A}$		-	2.6	-	S
<b>Dynamic <sup>b</sup></b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 10\text{ V}, f = 1\text{ MHz}$	-	27	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$			-	19	-	
Reverse Transfer Capacitance	$C_{rss}$			-	7	-	
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{GS} = 4.5\text{ V}$	$V_{DS} = 10\text{ V}, I_D = 1.2\text{ A}$	-	1	1.25	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			-	0.14	-	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	0.27	-	
Gate Resistance <sup>d</sup>	$R_g$	f = 1 MHz		1.5	3	4.5	k $\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 20\text{ }\Omega$ $I_D = 0.5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		-	66	82	ns
Rise Time <sup>c</sup>	$t_r$			-	108	135	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			-	715	893	
Fall Time <sup>c</sup>	$t_f$			-	390	487	
<b>Source-Drain Diode Ratings and Characteristics <sup>b</sup></b>							
Pulsed Current <sup>a</sup>	$I_{SM}$			-	-	3	A
Forward Voltage	$V_{SD}$	$I_F = 0.5\text{ A}, V_{GS} = 0$		-	0.8	1.2	V

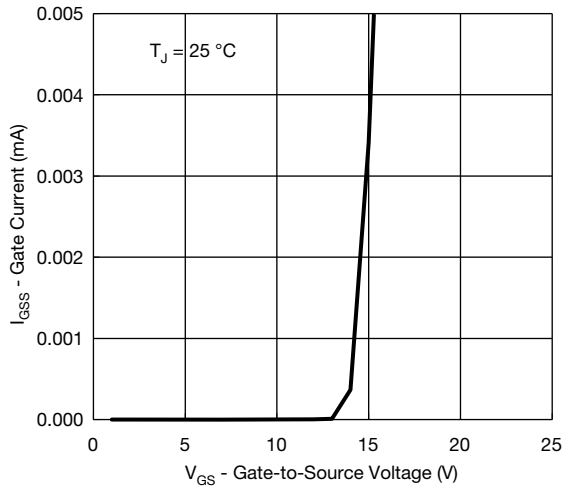
**Notes**

- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.
- Gate is obscured by ESD network series resistance and cannot be tested directly.

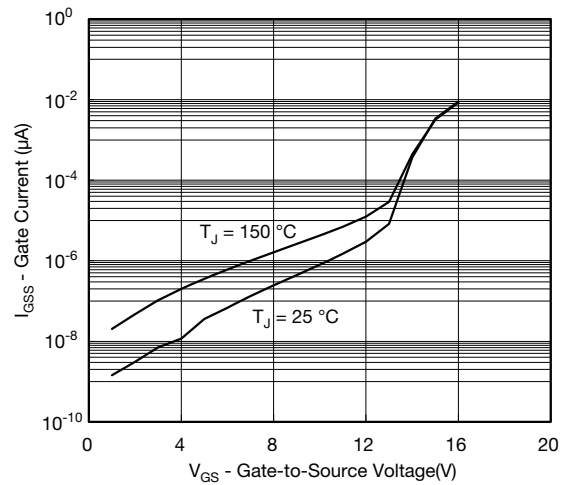
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



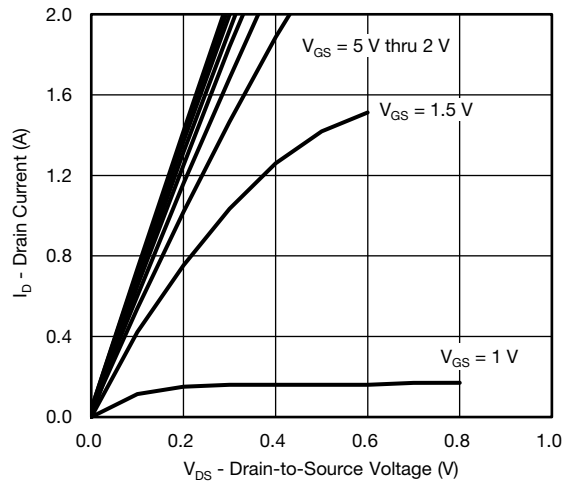
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



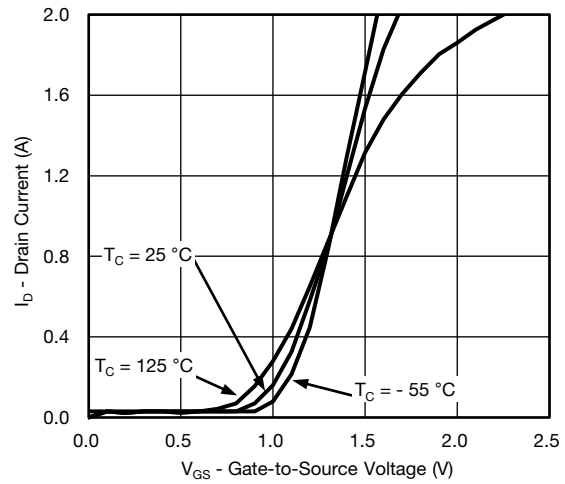
Gate Current vs. Gate-Source Voltage



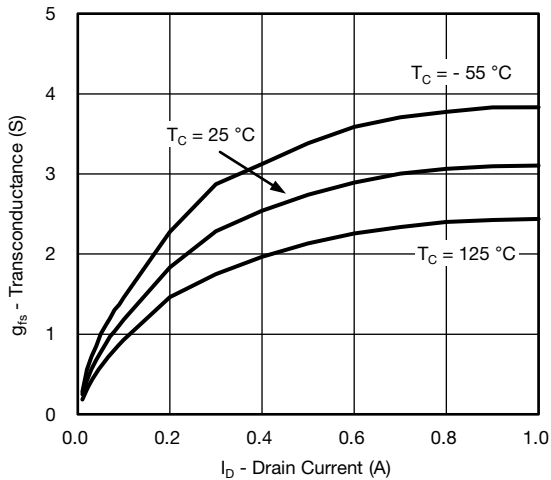
Gate Current vs. Gate-Source Voltage



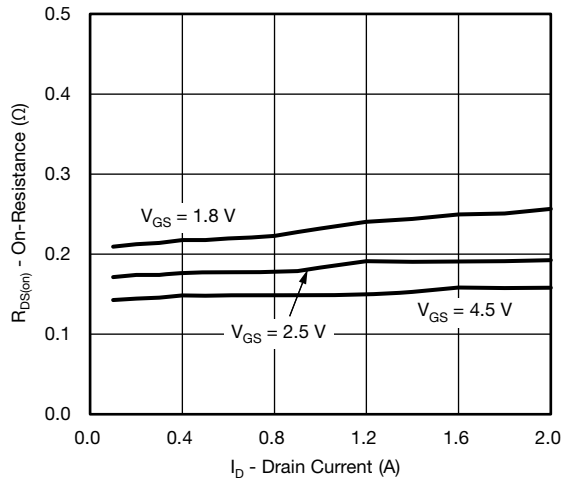
Output Characteristics



Transfer Characteristics



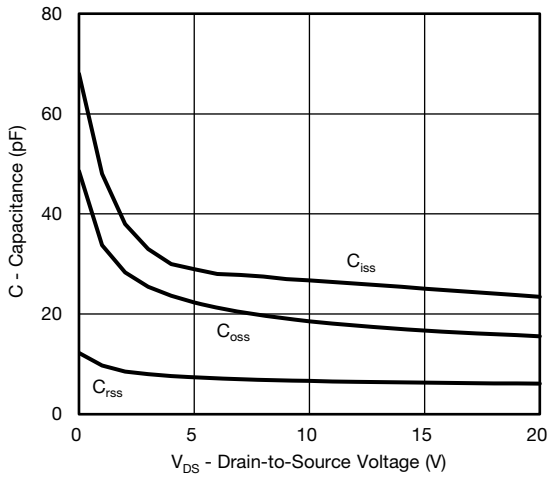
Transconductance



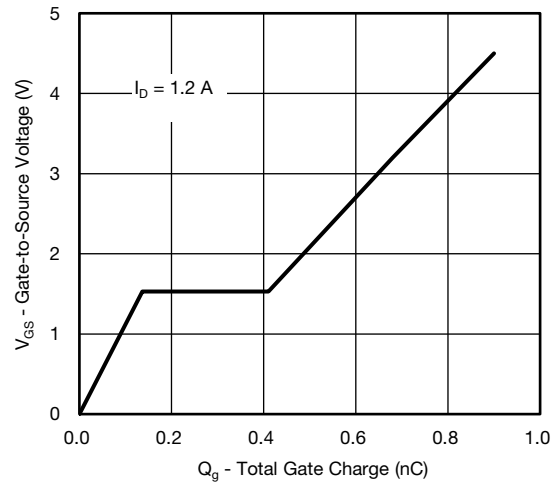
On-Resistance vs. Drain Current



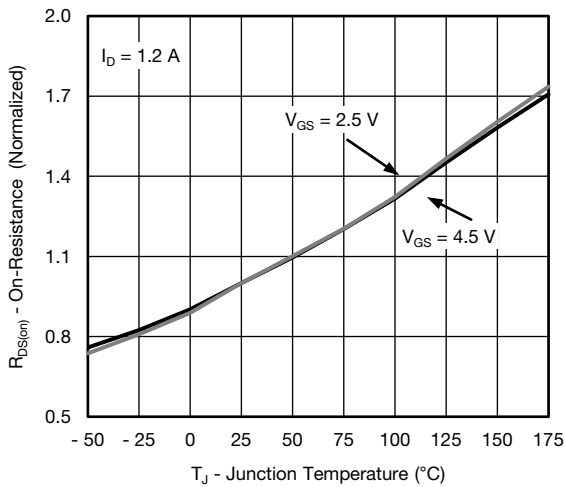
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



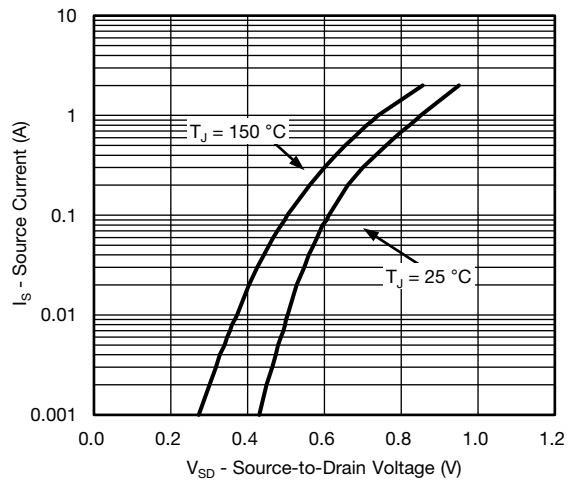
Capacitance



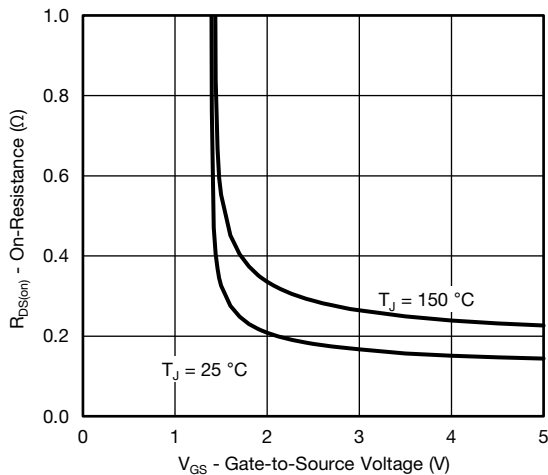
Gate Charge



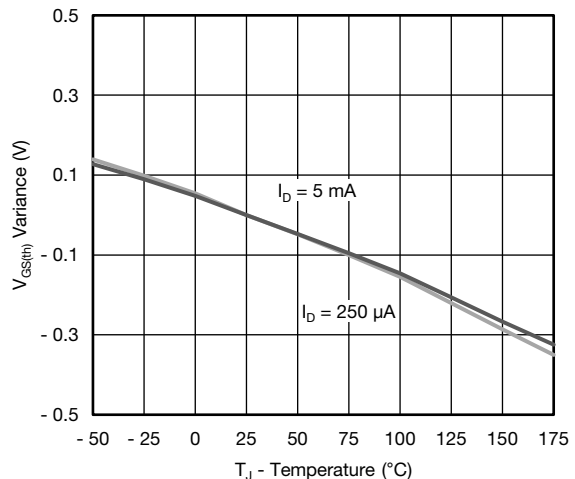
On-Resistance vs. Junction Temperature



Source Drain Diode Forward Voltage



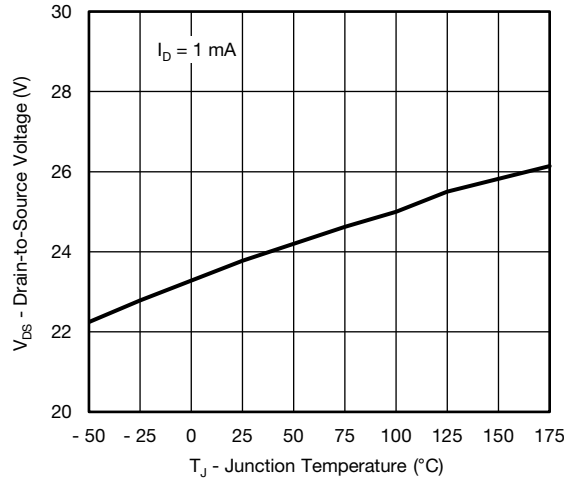
On-Resistance vs. Gate-to-Source Voltage



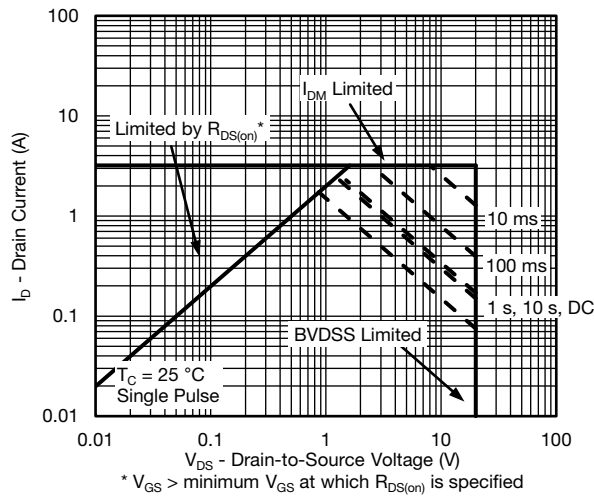
Threshold Voltage



**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



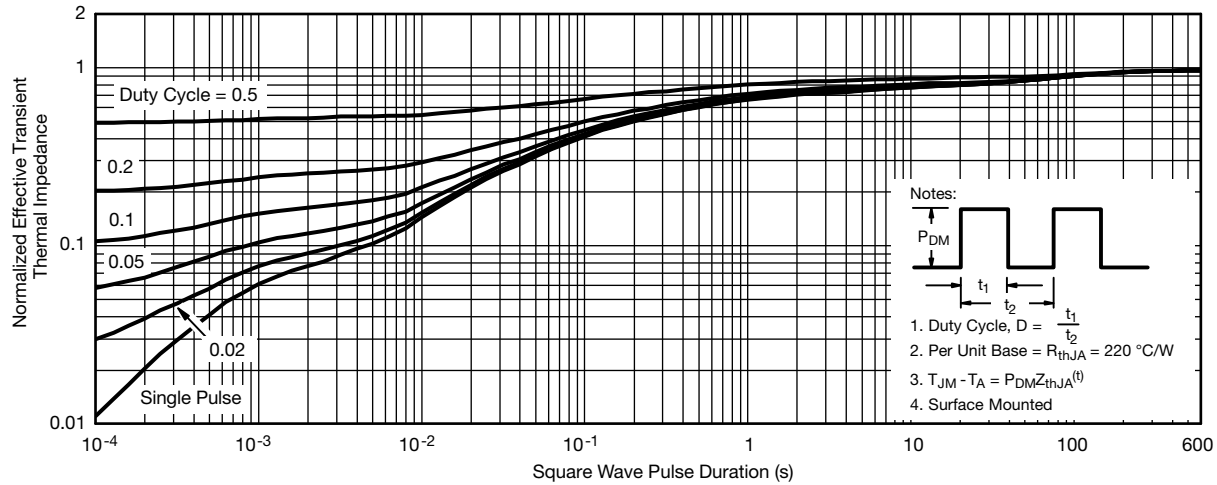
**Drain Source Breakdown vs. Junction Temperature**



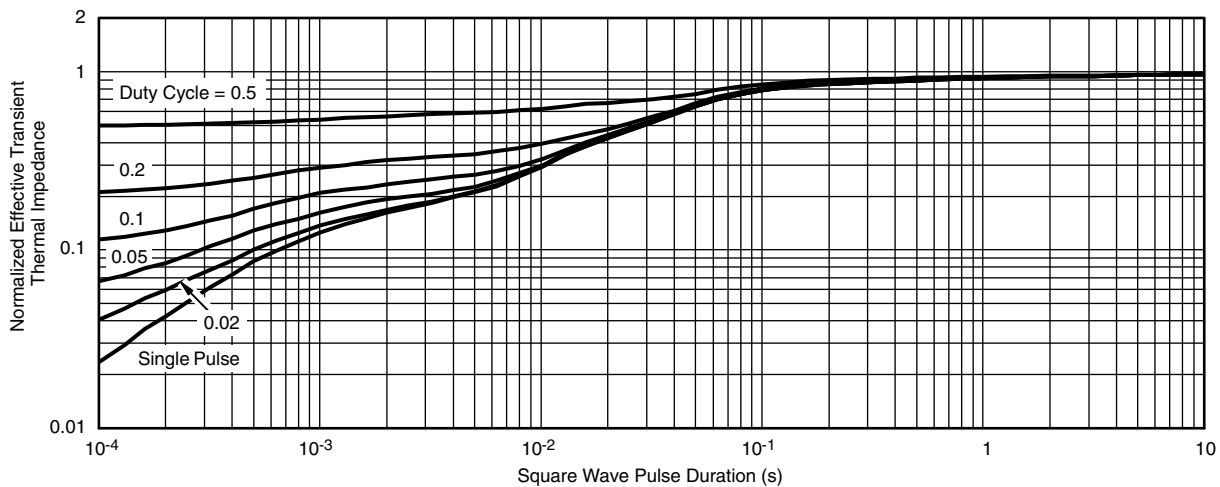
**Safe Operating Area**



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

**Note**

- The characteristics shown in the two graphs
    - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
    - Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)
- are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?62983](http://www.vishay.com/ppg?62983).



**SC-70: 6-LEADS**



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	-	1.10	0.035	-	0.043
A <sub>1</sub>	-	-	0.10	-	-	0.004
A <sub>2</sub>	0.80	-	1.00	0.031	-	0.039
b	0.15	-	0.30	0.006	-	0.012
c	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E <sub>1</sub>	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e <sub>1</sub>	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01  
DWG: 5550

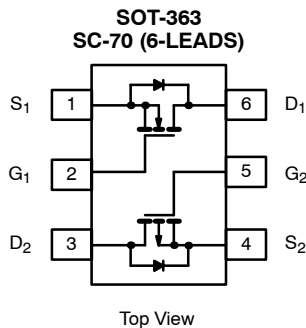
# Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance

## INTRODUCTION

The new dual 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the dual-channel version.

## PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration. Both n- and p-channel devices are available in this package – the drawing example below illustrates the p-channel device.

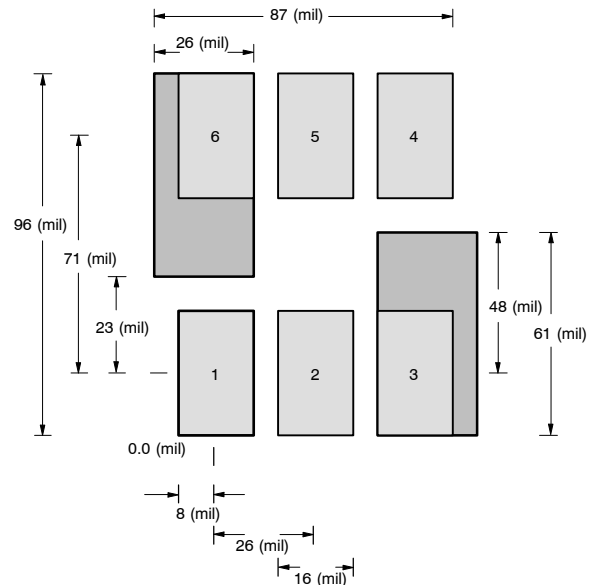


Top View  
**FIGURE 1.**

For package dimensions see outline drawing SC-70 (6-Leads) (<http://www.vishay.com/doc?71154>)

## BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>) for the SC-70 6-pin basic pad layout and dimensions. This pad pattern is sufficient for the low-power applications for which this package is intended. Increasing the drain pad pattern (Figure 2) yields a reduction in thermal resistance and is a preferred footprint.



**FIGURE 2.** SC-70 (6 leads) Dual

## EVALUATION BOARD FOR THE DUAL-CHANNEL SC70-6

The 6-pin SC-70 evaluation board (EVB) shown in Figure 3 measures 0.6 in. by 0.5 in. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows for examination from the outer pins to the 6-pin DIP connections, permitting test sockets to be used in evaluation testing.

The thermal performance of the dual 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was then repeated using the 1-inch<sup>2</sup> PCB with dual-side copper coating.

A helpful way of displaying the thermal performance of the 6-pin SC-70 dual copper leadframe is to compare it to the traditional Alloy 42 version.



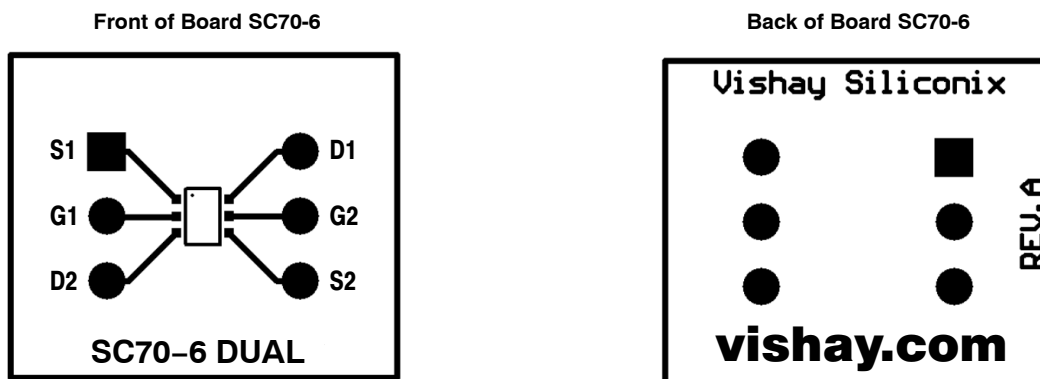


FIGURE 3.

**THERMAL PERFORMANCE**

**Junction-to-Foot Thermal Resistance (the Package Performance)**

Thermal performance for the dual SC-70 6-pin package is measured as junction-to-foot thermal resistance, in which the “foot” is the drain lead of the device as it connects with the body. The junction-to-foot thermal resistance for this device is typically 80°C/W, with a maximum thermal resistance of approximately 100°C/W. This data compares favorably with another compact, dual-channel package – the dual TSOP-6 – which features a typical thermal resistance of 75°C/W and a maximum of 90°C/W.

**Power Dissipation**

The typical  $R_{\theta JA}$  for the dual-channel 6-pin SC-70 with a copper leadframe is 224°C/W steady-state, compared to 413°C/W for the Alloy 42 version. All figures are based on the 1-inch<sup>2</sup> FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at varying ambient temperatures.

**Alloy 42 Leadframe**

ALLOY 42 LEADFRAME	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$
$P_D = \frac{150^{\circ}C - 25^{\circ}C}{413^{\circ}C/W}$	$P_D = \frac{150^{\circ}C - 60^{\circ}C}{413^{\circ}C/W}$
$P_D = 303 \text{ mW}$	$P_D = 218 \text{ mW}$

COOPER LEADFRAME	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$
$P_D = \frac{150^{\circ}C - 25^{\circ}C}{224^{\circ}C/W}$	$P_D = \frac{150^{\circ}C - 60^{\circ}C}{224^{\circ}C/W}$
$P_D = 558 \text{ mW}$	$P_D = 402 \text{ mW}$

Although they are intended for low-power applications, devices in the 6-pin SC-70 dual-channel configuration will handle power dissipation in excess of 0.5 W.

**TESTING**

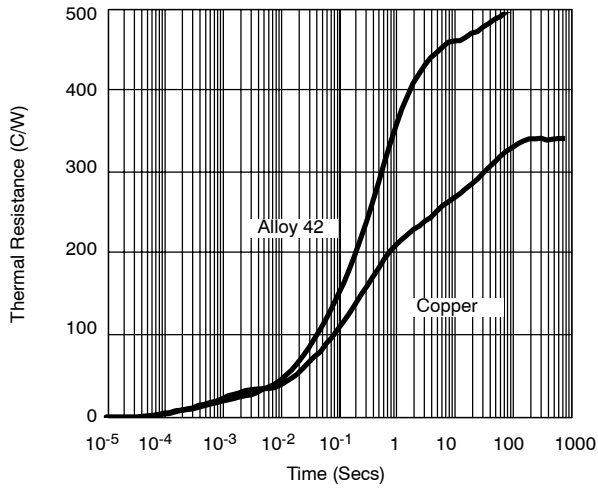
To further aid the comparison of copper and Alloy 42 leadframes, Figures 4 and 5 illustrate the dual-channel 6-pin SC-70 thermal performance on two different board sizes and pad patterns. The measured steady-state values of  $R_{\theta JA}$  for the dual 6-pin SC-70 with varying leadframes are as follows:

LITTLE FOOT 6-PIN SC-70		
	Alloy 42	Copper
1) Minimum recommended pad pattern on the EVB board (see Figure 3).	518°C/W	344°C/W
2) Industry standard 1-inch <sup>2</sup> PCB with maximum copper both sides.	413°C/W	224°C/W

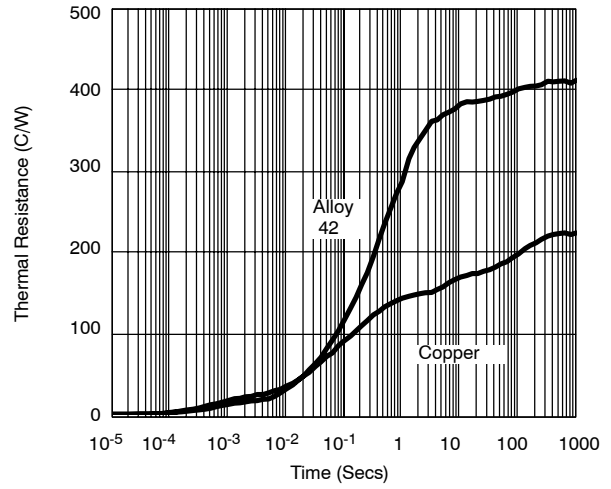
The results indicate that designers can reduce thermal resistance ( $\theta_{JA}$ ) by 34% simply by using the copper leadframe device as opposed to the Alloy 42 version. In this example, a 174°C/W reduction was achieved without an increase in board area. If an increase in board size is feasible, a further 120°C/W reduction can be obtained by utilizing a 1-inch<sup>2</sup>. PCB area.

The Dual copper leadframe versions have the following suffix:

Dual: Si19xxEDH  
 Compl.: Si15xxEDH

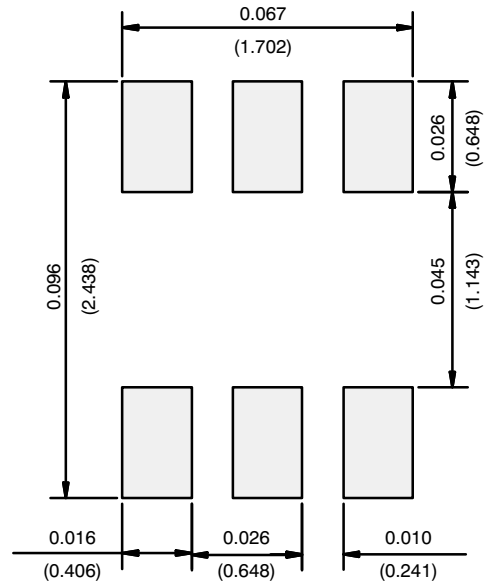


**FIGURE 4.** Dual SC70-6 Thermal Performance on EVB



**FIGURE 5.** Dual SC70-6 Comparison on 1-inch<sup>2</sup> PCB

## RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



## Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.