VRPower® Integrated Power Stage Solution

By Ron Vinsant

VRPower® products are integrated power stage solutions optimized for high-performance synchronous buck applications. These devices offer high power conversion efficiency and high power density with low electrical parasitics due to both excellent silicon (MOSFETs and drivers) and packaging design techniques. The devices are available in Vishay's proprietary 4.5 mm by 3.5 mm package for 30 A applications, and the industry-standard 5 mm by 5 mm thermally enhanced MLP package for 60 A applications.

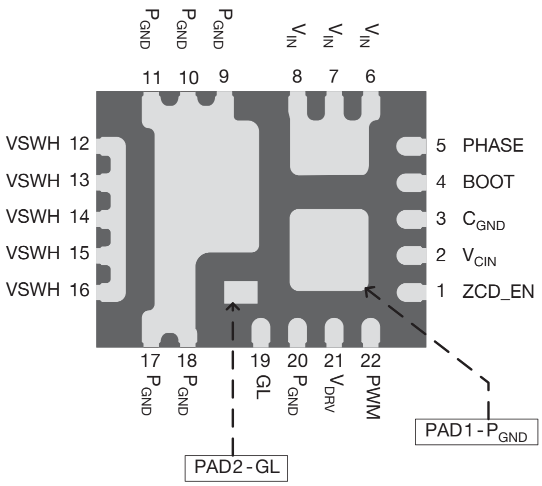

Fig. 1 - 3.5 mm by 4.5 mm package

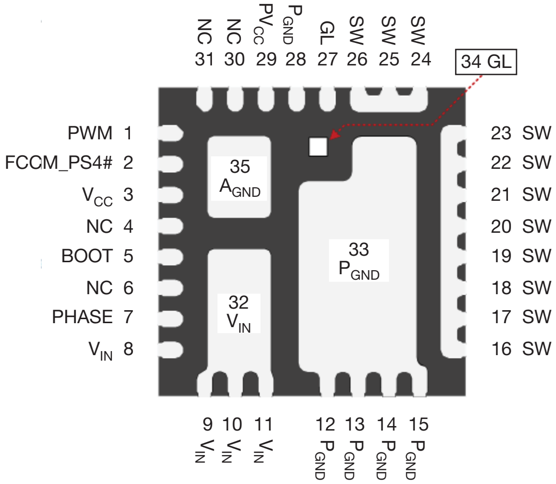

Fig. 2 - 5 mm by 5 mm package

VRPower devices are primarily intended for use in applications with 12 V inputs and < 2 V outputs. The power devices - MOSFETs - are asymmetrical to match the expected duty ratios in the intended operating range. The internal drivers are then matched to the MOSFETs to maximize efficiency.

This application document is meant to be used as a guide to the performance possibilities of some of the most popular Vishay VRPower products. We will cover efficiency and power loss over the operating frequency range of 400 kHz to 1 MHz. The 3.5 mm by 4.5 mm, 30 A device (SiC530) will be covered first, followed by the 5 mm by 5 mm, 60 A device (SiC620). Future application documents will cover EMC, boot resistor, capacitor, and thermal issues, and how they are affected by layout.

The "rated current" of a VRPower device is not an indicator of its performance under steady-state conditions. While it can be misleading, it is intended to be a guide for those applications where there are transient operating conditions requiring high peak currents, such as processors.

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SiC530: 3.5 mm by 4.5 mm, 30 A

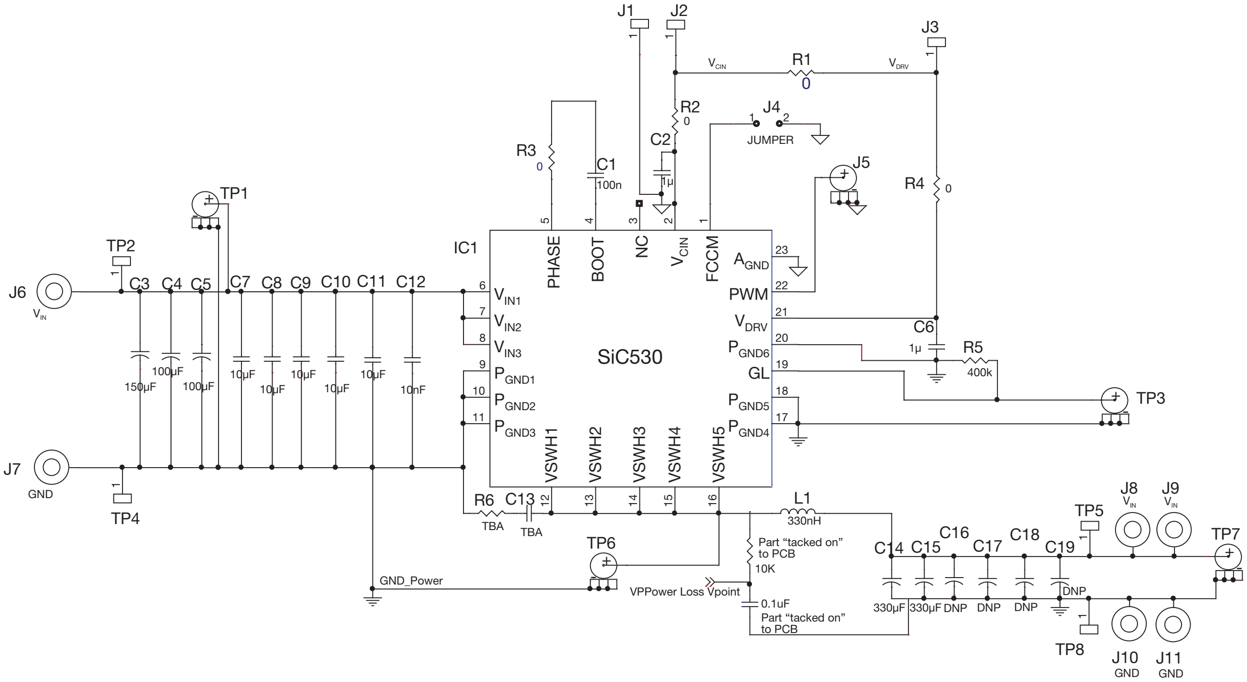
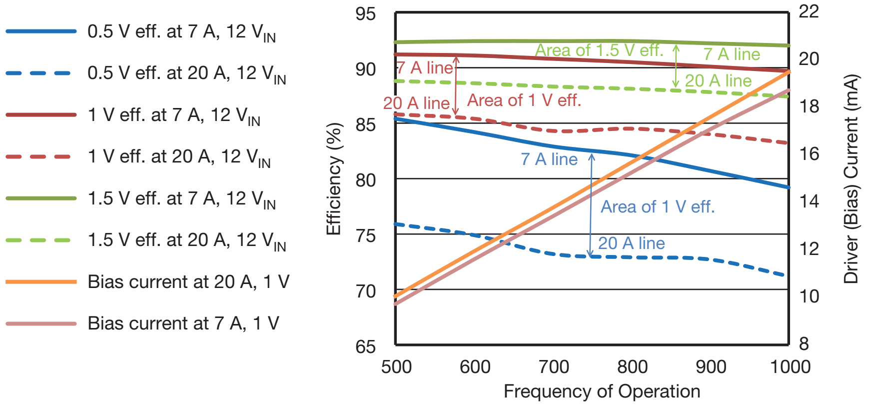


Fig. 3 - SiC530: 3.5 mm by 4.5 mm test board schematic

EFFICIENCY, POWER LOSS, AND OPERATING FREQUENCY

The SiC530 is normally used over a frequency operating range of 500 kHz to 1 MHz. The graph below shows efficiency and bias power requirements over that operating range.



Conditions:
12 V_{IN}, 0 Ω boot R
0.39 μH, HC8-R39-R L
3 x 220 μF, 10 V polymer caps, 6 mΩ
Ambient from 23 °C to 27 °C
Efficiency for power stage only;
no driver power is included,
MLP 5 x 5 test board (six layer)
Convection airflow, 50 % RH.

Fig. 4 - Area of efficiency from peak efficiency point (7 A) to max. current (20 A) for three different operating points: 0.5 V, 1 V, and 1.5 V outputs with 5 V MOSFET drive bias currents

Although the SiC530 is rated at 25 A, our testing was limited to 20 A for Fig. 4 due to our PCB construction being only six layers. Since the PCB supplies much of the heatsinking for the SiC530, its thermal properties are critical.

We are often asked about the expected performance of a SiC530. It is a difficult question to answer in general, and even more difficult to answer with any precision. It is instructive, however, to look at some typical examples that are in common use. One such example is shown below in Fig. 5.

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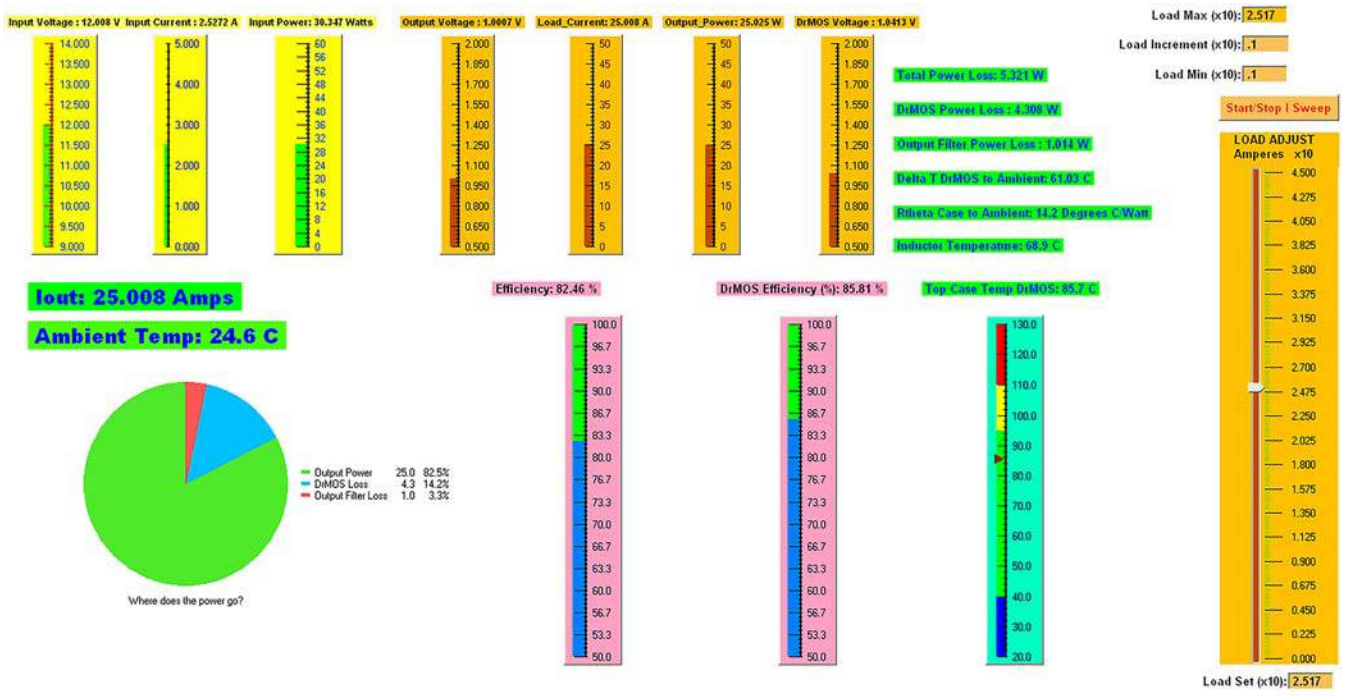


Input Voltage : 12.008 V
Input Current : 2.5272 A
Input Power: 30.347 Watts
Output Voltage : 1.0007 V
Load_Current: 25.008 A
Output_Power: 25.025 W
DrMOS Voltage : 1.0413 V
Total Power Loss: 5.321 W
DrMOS Power Loss : 4.308 W
Output Filter Power Loss : 1.014 W
Delta T DrMOS to Ambient: 61.03 C
Rtheta Case to Ambient: 14.2 Degrees C/Watt
Inductor Temperature: 68.9 C
Iout: 25.008 Amps
Ambient Temp: 24.6 C
Efficiency: 82.46 %
DrMOS Efficiency (%): 85.81 %
Top Case Temp DrMOS: 85.7 C
Load Max (x10): 2.517
Load Increment (x10): .1
Load Min (x10): .1
Load Set (x10): 2.517

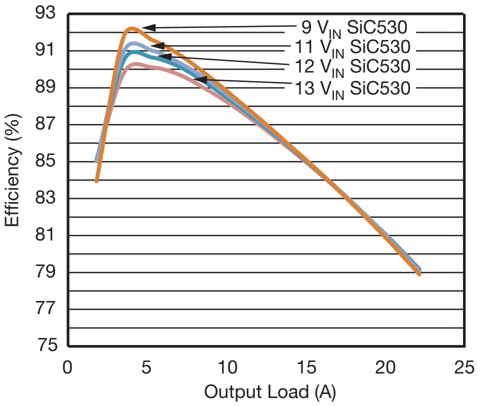
Output Power	25.0	82.5%
DrMOS Loss	4.3	14.2%
Output Filter Loss	1.0	3.3%

Fig. 5 - “Dashboard” example of the typical performance of a SiC530 with a 1 V output at 500 kHz

In Fig. 5 we can observe some of the expected operating temperatures of key components and their corresponding power losses when using a SiC530 in a 12 V_{IN}, 1 V_{OUT}, 500 kHz application at 25 A.

The term “filter loss” refers to the combination of the filter cap losses and inductor losses. These losses are typically dominated by the inductor.

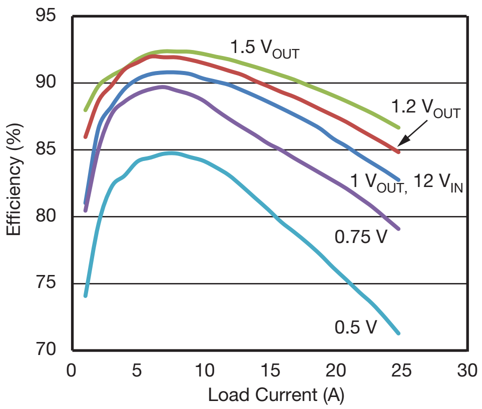
In Fig. 6 below we can see efficiency at higher frequency operation.



Conditions:
Ambient: 23 °C to 28 °C
0.9 V_{OUT}, 800 kHz
0.22 μH, 3.9 mΩ DCR
(custom)
100 μF x 5R, 1206 caps (13 μA)
220 μF POSCAPS (4)
Single-phase, 0 Ω boot R
SiC530 temp (on top) 65.3 °C at 20 A with 13 V_{IN}
SiC530 efficiency only; does not
include all bias power for board
and controller

Fig. 6 - SiC530 800 kHz, 0.9 V_{OUT} single-phase efficiency vs. load for different V_{IN}

In Fig. 7 below we show operation at 500 kHz.



Conditions: 12 V_{IN}, 0 Ω boot R
Inductor: Coiltronics, HC-R39-R, 0.39 μH,
1.55 mΩ DCR
3 x 220 μF, 10 V, polymer cap, 6 mΩ ESR
Ambient: 23 °C to 27 °C
Efficiency for power stage only; no driver power
Convection airflow, 50 % RH
Six-layer PCB

Fig. 7 - Efficiency of SiC530 at 500 kHz for 12 V_{IN} with 0.5 V to 1.5 V output voltage vs. load current

SiC620: 5 mm by 5 mm, 60 A

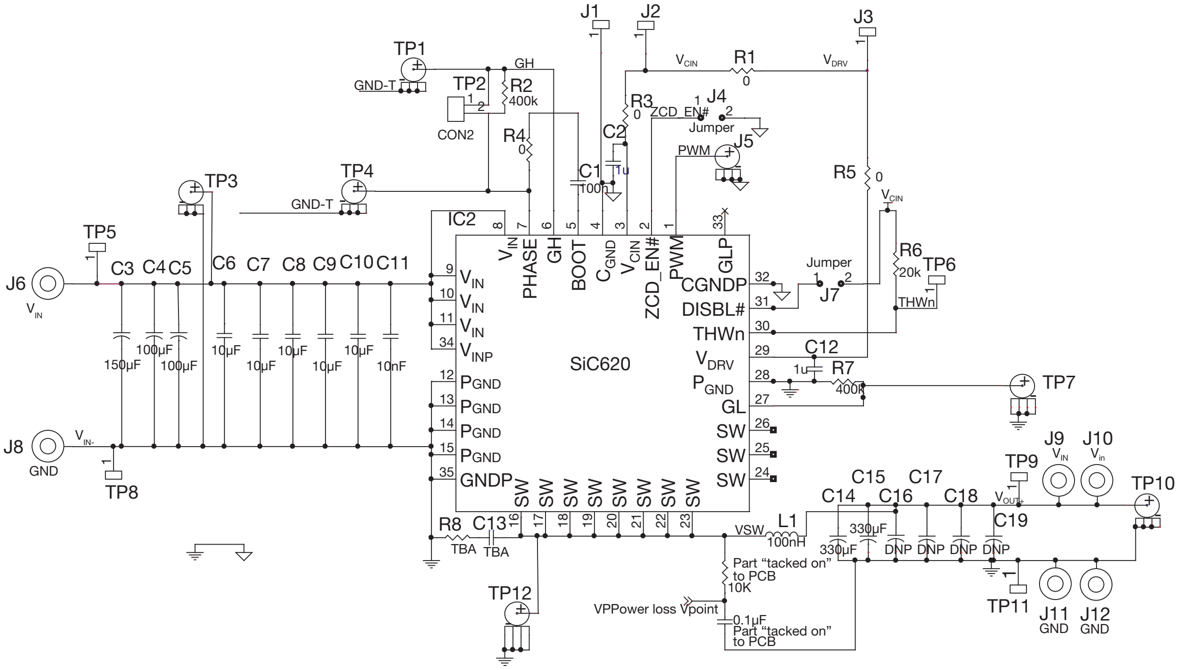
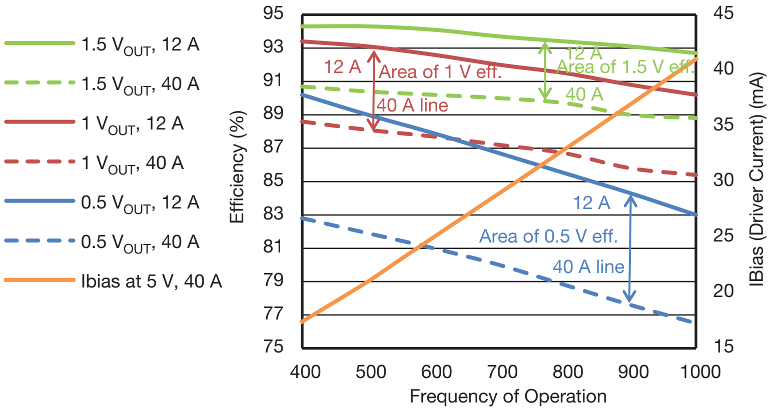


Fig. 8 - SiC620: 5 mm by 5 mm test board schematic

EFFICIENCY, POWER LOSS, AND OPERATING FREQUENCY

The SiC620 is normally used over a frequency operating range of 400 kHz to 1 MHz. The graph below shows efficiency and bias power requirements over that operating range.



Conditions: 12 V_{IN}, 0 Ω boot R
Inductor: Coiltronics, HC8-R39-R, 0.39 µH, 1.55 mΩ DCR
3 x 220 µF, 10 V, polymer cap, 6 mΩ ESR
Ambient: 23 °C to 27 °C
Efficiency for power stage only; no driver power
Convection airflow, 50 % RH
Six-layer PCB

Fig. 9 - Area of efficiency from peak efficiency point (12 A) to max. current (40 A) for three different operating points: 0.5 V, 1 V, and 1.5 V outputs with 5 V MOSFET drive bias currents

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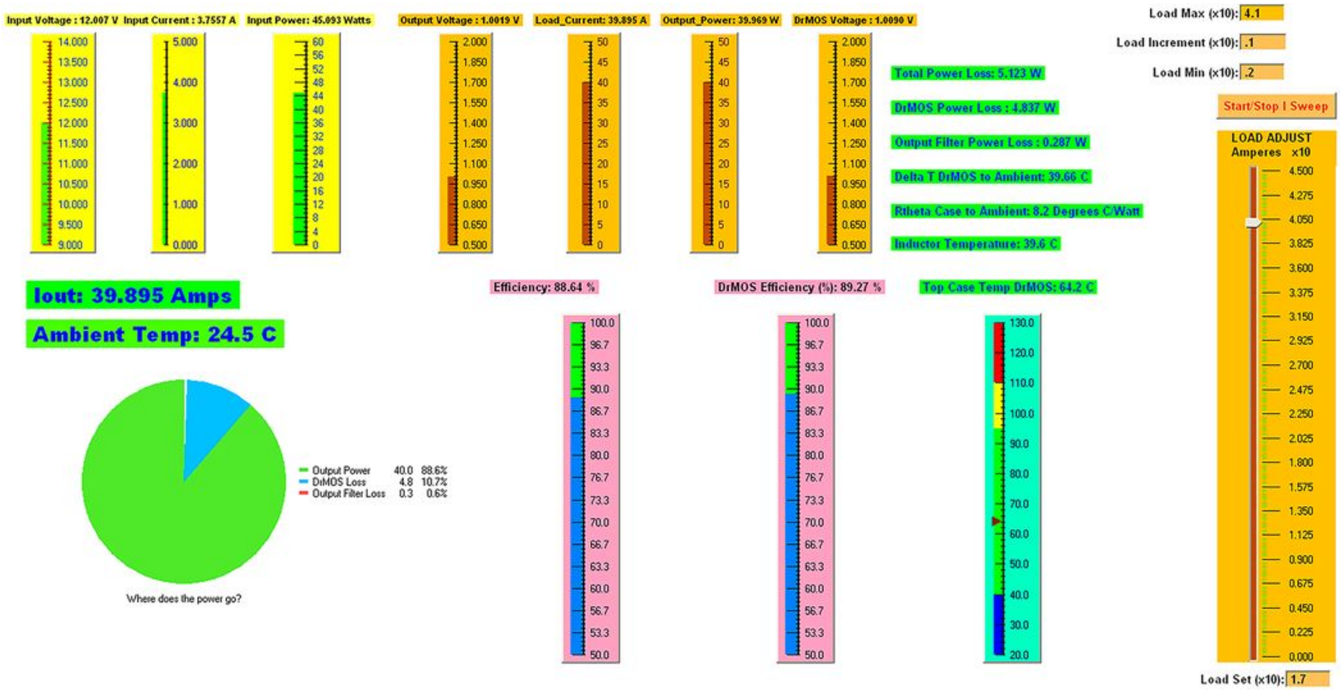

Input Voltage : 12.007 V
Input Current : 3.7557 A
Input Power: 45.093 Watts
Output Voltage : 1.0019 V
Load_Current: 39.895 A
Output_Power: 39.969 W
DrMOS Voltage : 1.0090 V
Total Power Loss: 5.123 W
DrMOS Power Loss : 4.837 W
Output Filter Power Loss : 0.287 W
Delta T DrMOS to Ambient: 39.66 C
Rtheta Case to Ambient: 8.2 Degrees C/Watt
Inductor Temperature: 39.6 C
Load Max (x10): 4.1
Load Increment (x10): .1
Load Min (x10): .2
Iout: 39.895 Amps
Ambient Temp: 24.5 C
Efficiency: 88.64 %
DrMOS Efficiency (%): 89.27 %
Top Case Temp DrMOS: 64.2 C
Load Set (x10): 1.7

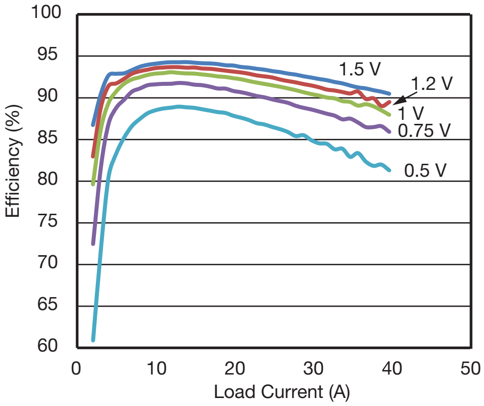
Output Power	40.0	88.6%
DrMOS Loss	4.8	10.7%
Output Filter Loss	0.3	0.6%

Fig. 10 - “Dashboard” example of the typical performance of the SiC620 with a 40 A, 1 V output at 412 kHz

In Fig. 10 we can observe some of the expected operating temperatures of key components and their corresponding power losses when using an SiC620 in a 12 V_{IN}, 1 V_{OUT}, 412 kHz application at 40 A. Unlike the SiC530 tests, the SiC620 tests were run with some airflow, as this would be the normal environment in higher-power applications.

The term “filter loss” is the combination of the filter cap losses and inductor losses. These losses are typically dominated by the inductor; output filter capacitors are a very small loss term in most applications.

In Fig. 11 below we show operation at 500 kHz.



Conditions:
12 V_{IN}, 0 Ω boot R, 500 kHz
0.25 μH, 744309025 Wurth
3 x 220 μF, 10 V, polymer caps, 6 mΩ
Ambient: 23 °C to 27 °C
Efficiency for power stage only;
no driver power is included
MLP 5 x 5 test board (six-layer)
Convection airflow, 50 % RH

Fig. 11 - Efficiency of SiC620 at 500 kHz for 12 V_{IN} with 0.5 V to 1.5 V output voltage vs. load current

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ISSUES RELATED TO ALL VRPower PRODUCTS

Inductor Power Loss

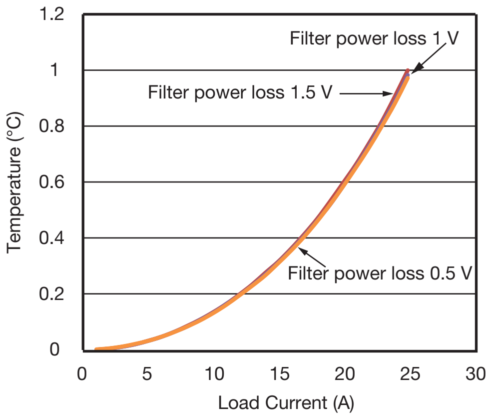

Fig. 12 - Output filter power loss for three different operating points (0.5 V, 1 V, and 1.5 V) for an SiC530

This shows that in general, the power loss in the filter (L1 and C14 through C19, referring to Fig. 3) is dominated by the DC loss term and not AC (magnetic core) losses. This would leave one to believe that the temperature of the inductor would only change due to load and not V_{OUT}.

This is not true, however. The inductor temperature does change with V_{OUT}, as we can see below.

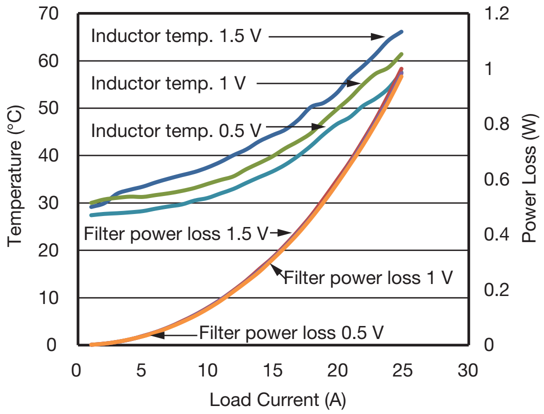

Fig. 13 - Output filter power loss and temperature for three different operating points - 0.5 V, 1 V, and 1.5 V

If a good electrical layout is achieved, the inductor is always placed as close as possible to the V_{SW} pins of the SiC530 to minimize inductance in the path, which causes ringing that places added stress on the device.

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Here is an example PCB layout showing how close the two components should be.

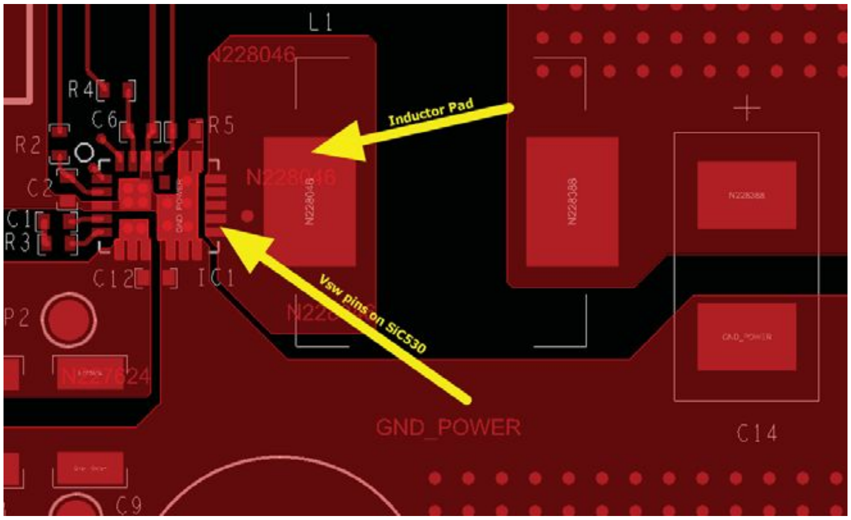


Fig. 14 - **SiC530 evaluation board layout showing the close proximity of an inductor to the SiC530**

Being close to the switching device allows the inductor to absorb heat from the SiC530; in other words it is a heatsink, and thus is very important to the thermal design of the regulator. If the inductor is placed in airflow it will help keep temperatures down. Keeping other PCB-mounted components out of the airflow path passing the inductor is always helpful.

Below, we can observe that losses, and therefore temperature rise, in the SiC530 are not linearly proportional to V_{OUT} for any specific load point.

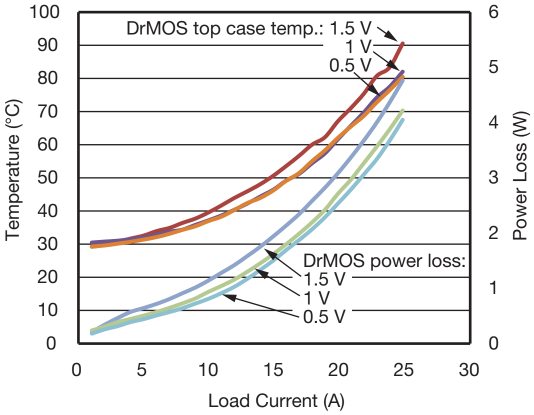


Fig. 15 - **SiC530 power loss and top case temperature**

This non-linearity shows that while a 1.5 V, 25 A output might not meet required design goals due to temperature rise, at 1 V such a design might be acceptable due to the lower operating temperature of the SiC530.

Please note we are using the same inductor for all outputs for this test. In a typical system design the inductor value would change depending on load specifications such as ripple and transient response. Since the peak value of current in the inductor is one of the parameters that determines switching loss in the high-side MOSFET, results might be different for lower voltages with smaller-value inductors.

Inductor Core Loss

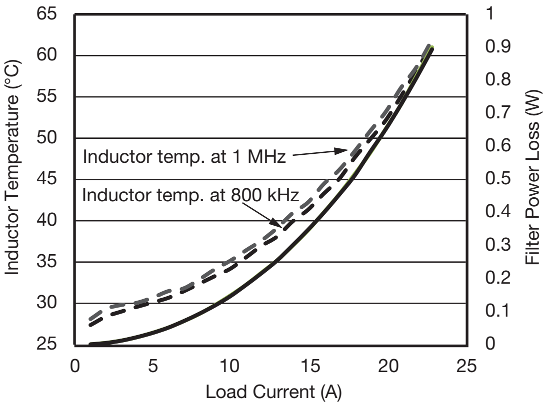
It is often stated that increasing the switching frequency is not prudent as it will increase magnetic losses. If the value of the inductor does not change and the frequency increases, core losses actually go down, not up, as the delta B (flux swing) in the inductor is less.

A typical model for core loss is shown below:

$PL = 492 \times B^{2.22} f^{1.32}$ for Magnetics Inc. high-flux 60 μ core material,

where PL is power loss, B is one half the peak-to-peak flux swing, and f is frequency. Note that the exponent for B is much greater than for f.

Below is an example (note there is little to no change in power loss in the inductor).



Circuit and conditions:
13 V_{IN}, 0.9 V_{OUT}, 0 Ω boot R
800 kHz and 1 MHz
0.22 μH, 8 mm x 8 mm
3 x 220 μF, 10 V, polymer cap,
6 mΩ ESR
Ambient: 23 °C to 27 °C
Power stage only; no driver power
CCM driver power is
SiC530 800K
15.3 mA at 5 V = 76.5 mW
SiC530 1 MHz
18.9 mA at 5 V = 94.5 mW

Fig. 16 - Inductor loss and temperature at two operating frequencies with the same inductor in an SiC530

The additional change in temperature of the inductor is, as we have shown above, due to the increased switching losses in the SiC530, and not inductor loss.

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Inductor Saturation

In some VRPower applications, space is critical and the largest component is most often the inductor. Due to its large size, it is the first component to be addressed in solving any space issues.

As the size of the inductor decreases, its ability to store energy decreases. This is dependent on a number of factors, such as magnetic material and operating temperature. If the saturation level of the inductor is exceeded, the currents in the VRPower MOSFETs will increase and cause additional power loss in the VRPower device.

Observing the current in the inductor with a current probe is a useful way of determining if the inductor is heading into saturation.

Below is an example of the normal operation of two inductors of the same type.

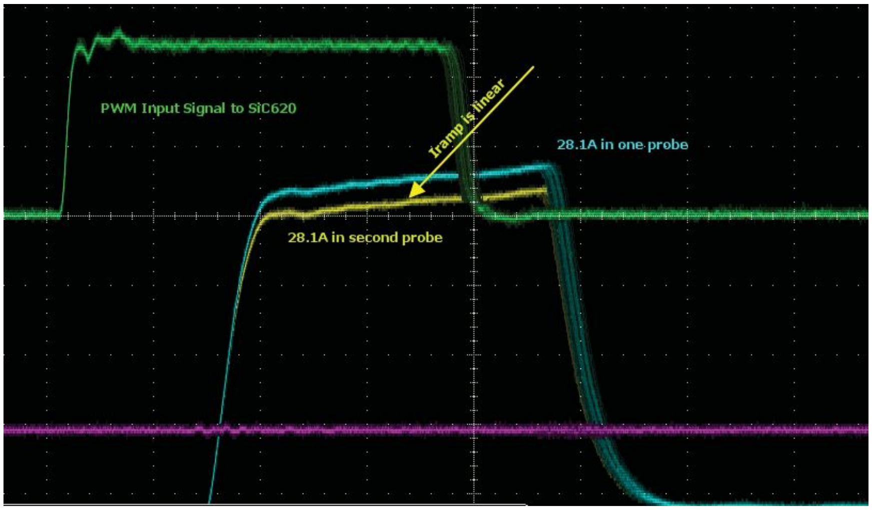

Fig. 17 - Normal inductor operation; linear current ramp

With only a small increment in current from 28.1 A to 30.27 A, we can see the current ramp becoming non-linear.

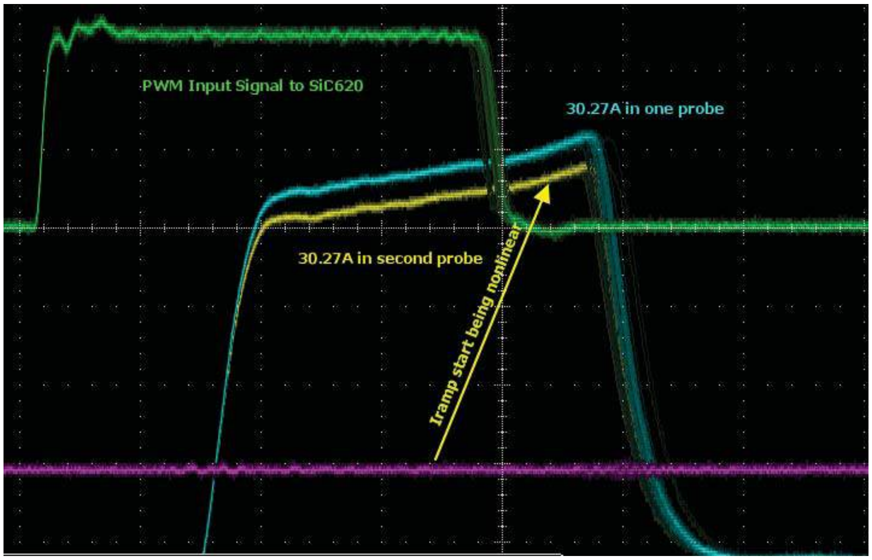

Fig. 18 - Border-line inductor operation; current ramp becoming non-linear

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With yet another small increment from 30.27 A to 32.2 A, we see a very large increase in peak current.

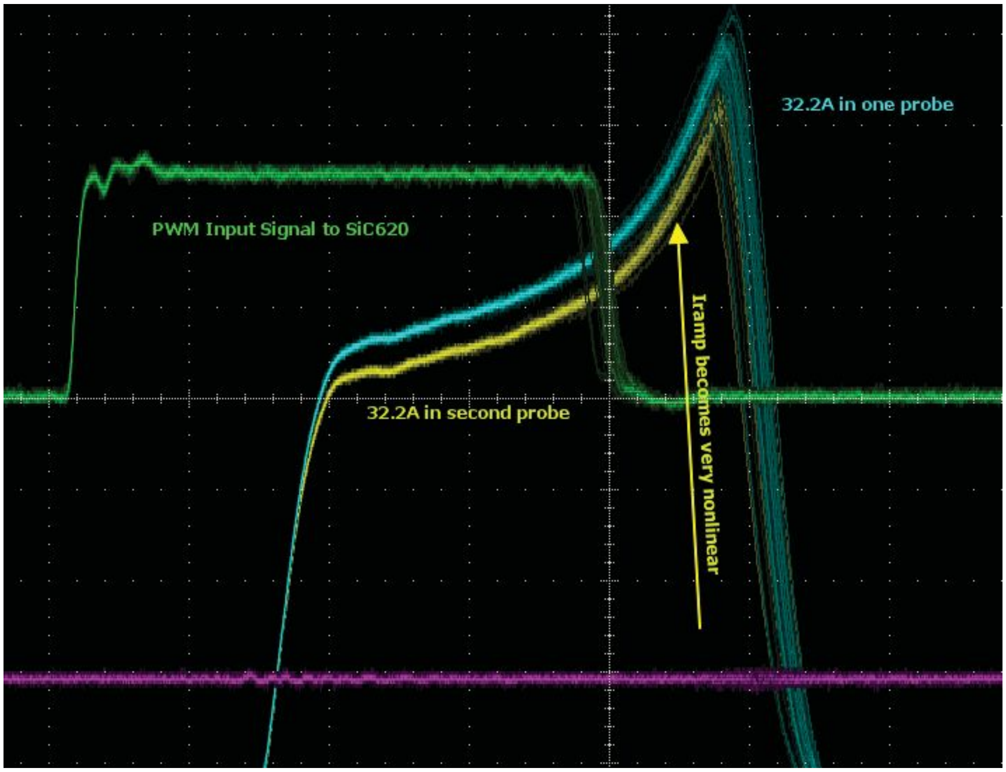

Fig. 19 - Saturated inductor operation; current ramp very non-linear

The peak current increases both conduction losses and switching losses in the high-side MOSFETs of the VRPower device. Operation in this region should be avoided due to increased stresses on the MOSFETs.

If the control system utilizes DCR current sensing, there is also the issue of inaccuracy of the current sense value due to the non-linearity of the value of L.

Another question that frequently arises is the effect of varying L on efficiency and power loss. There are many variables involved, such as PCB layout, physical and electrical size of the inductor, input voltage, boot resistor value, etc.

In Fig. 20 below, we show an example of what might be expected in a typical application for the SiC620. We use three different inductors. One is a 220 nH device with a “standard” height of 6 mm from Vishay; the second is a competitor’s 6 mm inductor, also of 220 nH; and an 8 mm, 300 nH inductor from Vishay. For any specific operating point, a large value of L results in a lower peak current decreasing the switching loss in the upper MOSFET and increasing efficiency. In addition, a larger physical size of L will result in additional heatsinking, further increasing efficiency and lowering operating temperatures. However, this increase in L will lower the ability of the control loop to respond to transient events.

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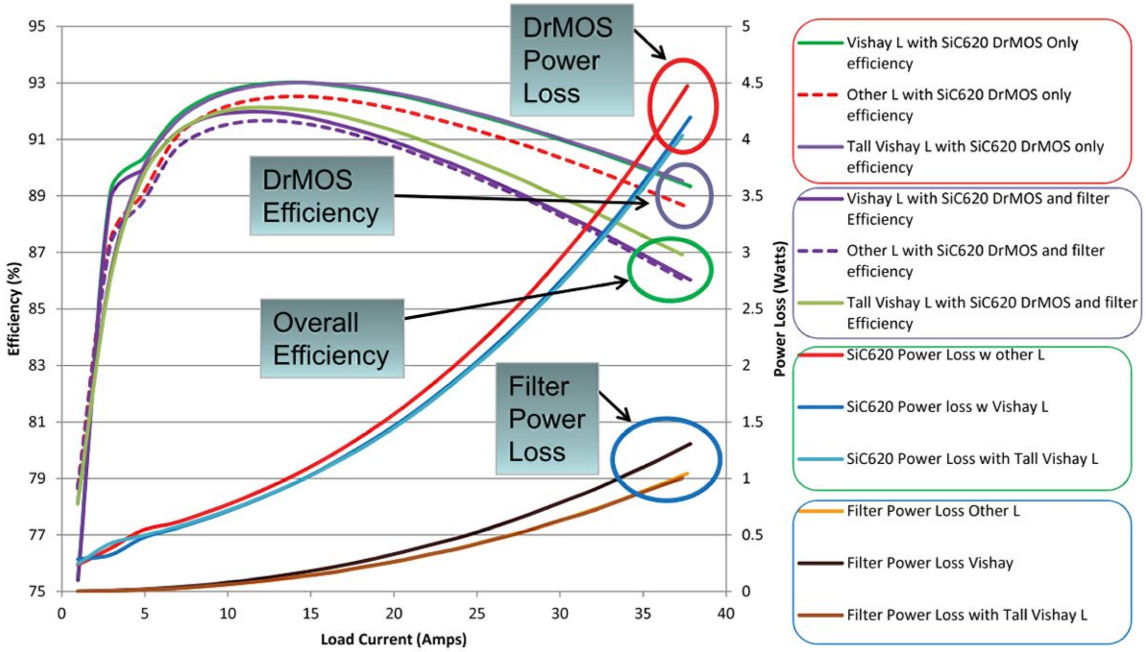


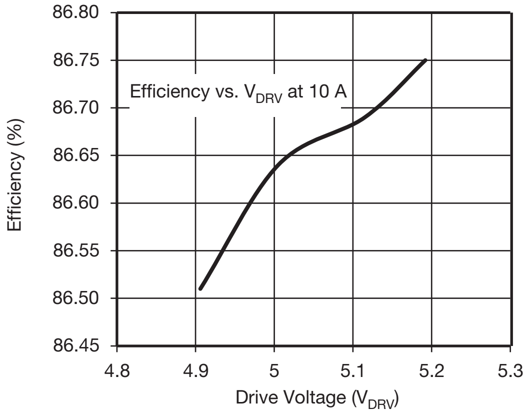
Conditions: 25 °C ambient, 220 nH L, tall Vishay L is 300 nH, 500 kHz, 12 V_{IN}, 0.9 V_{OUT}, 6 mΩ ESR, 100 µF caps x 3

Fig. 20 - Efficiency and power losses vs. load current for the SiC620 with different inductors

A design tool for inductor selection can be found here: www.vishay.com/inductors/calculator/calculator/

V_{DRV} Supply Voltage (MOSFET Gate Voltage)

VRPower devices use a 5 V drive for MOSFET enhancement. Varying this voltage over a small range will not substantially affect the efficiency of the devices. Fig. 21 below shows the effects on efficiency with changes in drive voltage.



Circuit and conditions:
13 V_{IN}, 0.9 V_{OUT}, 1.006 MHz
0.22 µH, 1 mΩ DCR L
3 x 220 µF, 10 V, polymer cap,
6 mΩ ESR
Ambient: 26 °C
Power stage only; no driver power
CCM driver power is
27.6 mA at 5 V = 138 mW
MLP 5 x 5 Test Board

Fig. 21 - Effect on efficiency due to drive voltage on SiC631 (3.5 mm x 4.5 mm)

Although these devices have a UVLO, it is prudent to design the system so that when in operation the VRPower device has a minimum value of 4.5 V for V_{DRV}.

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V_{CIN} Supply Voltage (Driver V_{CC} Voltage)

It is important that the supply voltage rail for the driver and the controller generating the PWM signal be the same. This requirement is due to the tri-state inputs on the PWM signal to the VRPower device.

Below is a simplified schematic of a VRPower device being driven by a system regulator.

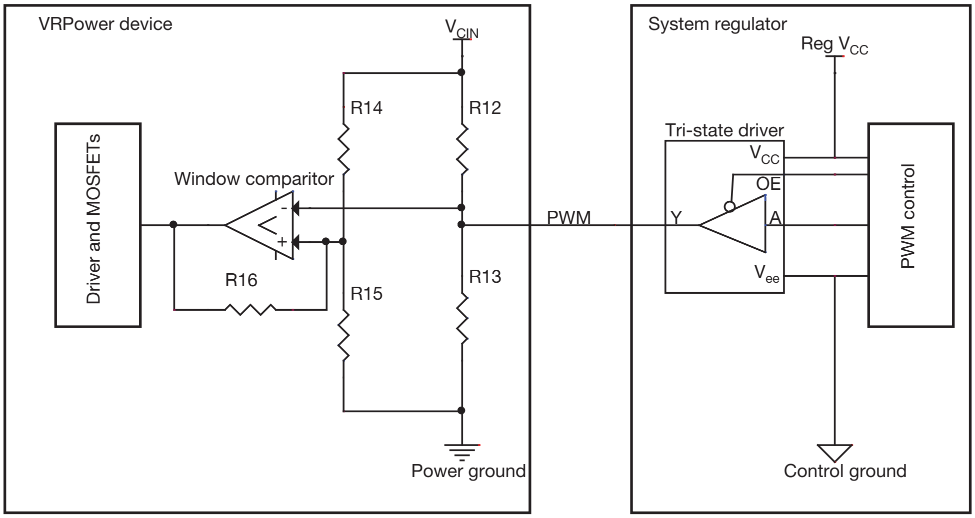

Fig. 22 - Simplified schematic of a VRPower device driven by a system regulator with separate grounds and supply rails

As V_{CIN} changes in magnitude, the threshold of the window comparator sensing the signal from the system regulator tri-state driver will change. If the system regulator's supply rail, Reg V_{CC}, is active before the VRPower device’s V_{CIN}, then there can be a region of operation as V_{CIN} rises where the device can have false triggering of the drivers and MOSFETs, leading to erratic behavior and possible device failure.

To a lesser extent this is also true of the ground paths. In order to reduce noise on the PWM signal, it is best not to have the grounds tied as shown in Fig. 22 above, but to tie both power rails and grounds of the system regulator and VRPower device together, as shown below.

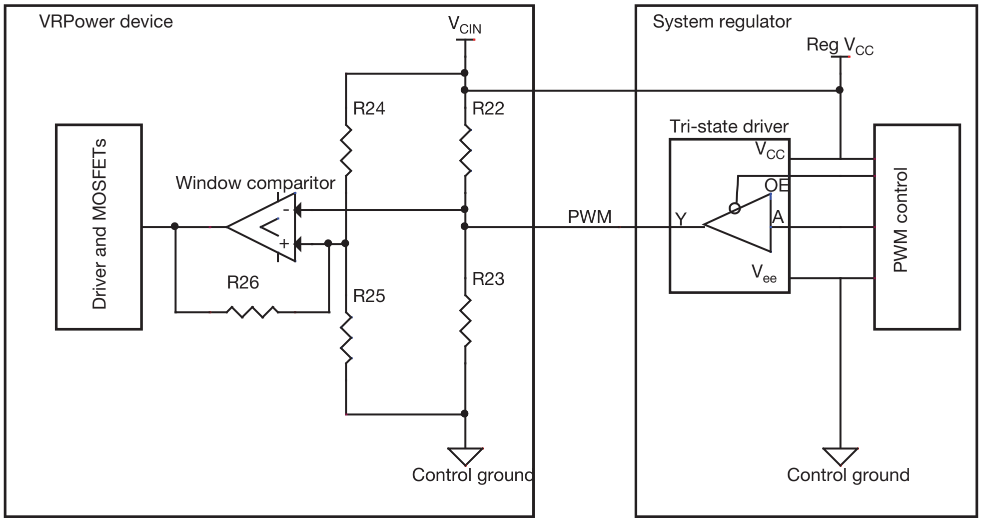

Fig. 23 - Simplified schematic of a VRPower device driven by a system regulator with properly tied grounds and supply rails

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Minimum on Time

At higher frequencies like 1 MHz and large input-voltage-to-output-voltage ratios, the parameter of minimum on time, $t_{PWM\_ON\_MIN}$, may be of concern. Since the ratio of V_{IN} to V_{OUT} when in continuous conduction mode is set by the ratio of the high-side MOSFET on time to the off time,

Time on = V_{OUT}/V_{IN} x 1 period; e.g. 0.5 V/12 = 0.0417 or a 4.17 % on time in 1 µs. This equates to 41.7 ns, which is less than the specified minimum PWM input of 50 ns.

Also consider this parameter on transient response. At load release, the PWM should be at as narrow a width as possible, or perhaps not be generated at all. When simulations are being run, this non-linearity must be considered.

CONCLUSIONS

1. Use the peak current rating as a "pulse" rating; not as a steady-state operating current specification.
2. The inductor is an important contributor to thermal, as well as electrical, design.
3. Do place the inductor close to the VRPower device in the PCB layout.
4. V_{OUT} has a large effect on operating temperature. Higher currents might be possible for applications where the operating temperature is the same, but since output voltage is lower, power loss is less, and therefore output current can be higher.
5. When selecting an inductor, be sure to assess the saturation parameters to minimize thermal and electrical stress on the VRPower device.
6. MOSFET drive voltage has little effect on overall efficiency, but should not drop below 4.5 V.
7. The control system and the VRPower device should be supplied from the same V_{CC} rail.
8. The control system ground should be tied to the analog ground of the VRPower device, not the power ground.
9. Take into account the minimum PWM input pulse when considering operating frequency in your design.