Reference Board User's Manual for SiC463, SiC464, SiC473, and SiC474 Synchronous Buck Regulators

DESCRIPTION

This reference board allows the user to evaluate the SiC463, SiC464, SiC473, and SiC474 microBUCK® regulators for their features and functionalities. It can also be a reference design for a user's application. The board is configured for 4.5 V to 50 V input. Output current capability is model dependent. The operating range may be modified by changing components such as the inductor, feedback resistor, and ripple injection networks.

The SiC46x and SiC47x family of microBUCK regulators is a wide input voltage high efficiency synchronous buck regulator with integrated high side and low side power MOSFETs. Its power stage is capable of supplying up to 10 A continuous current at up to 2 MHz switching frequency. These regulators produce an adjustable output voltage down to 0.8 V from 4.5 V to 60 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiC46x and SiC47x control architecture delivers ultrafast transient response with minimum output capacitance and tight ripple regulation at very light load. The device is stable with any type of output capacitor. The device also incorporates a power saving scheme that significantly increases light load efficiency.

This board has UVLO capability on the input rail and a user programmable soft start.

FEATURES

- Versatile
  - Single supply operation from 4.5 V to 60 V input voltage for SiC463 and SiC464, and 55 V for SiC473 and SiC474
  - Adjustable output voltage down to 0.8 V
  - Scalable solution from 2 A to 5 A
  - Support start-up with pre-bias output voltage
  - ± 1 % output voltage accuracy at -40 °C to +125 °C
- Highly efficient
  - 98 % peak efficiency
  - 5 µA supply current at shutdown
  - 250 µA operating current not switching
- Highly configurable
  - Adjustable switching frequency from 100 kHz to 2 MHz
  - Adjustable soft start and adjustable current limit
  - 3 modes of operation, forced continuous conduction, power save or ultrasonic
- Robust and reliable
  - Output over-voltage protection
  - Output under-voltage / short circuit protection with auto retry
  - Power good flag and over temperature protection
- Design support tool
  - PowerCAD online design simulation https://vishay.transim.com/landing.aspx
  - Inductor selection tool www.vishay.com/inductors/calculator/calculator/
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Industrial and automation
- Home automation
- Industrial computing
- Base station power supplies
- Wall transformer regulation
- Robotics
- Drones
- Battery management systems
- Power tools
- Vending, ATM, and slot machine

SPECIFICATIONS

This reference board allows the end user to evaluate the SiC463, SiC464, SiC473, and SiC474 microBUCK regulators for their features and functionalities. It can also be a reference design for a user's application. The board is configured for 4.5 V to 50 V input with different output voltages depending on the model number of the board. The operating range may be modified by changing components such as the inductor, feedback resistor, and ripple injection networks.

ORDERING INFORMATION		
BOARD PART NUMBER	MAXIMUM OUTPUT CURRENT	BOARD MARKING
SiC463EVB-B	4 A	UB46B
SiC464EVB-B	2 A	UB46B
SiC473EVB-B	5 A	UB46B
SiC474EVB-B	3 A	UB46B

BOARD CONFIGURATION TABLE

SiC463, SiC473 EVB TYPICAL PRE-DEFINED OPERATING CONFIGURATIONS				
V_{IN} (V)	V_{OUT} (V)	f_{sw} (kHz)	L (µH)	MAXIMUM I_{OUT} (A) SiC463 / SiC473
48.0	3.3	300	8.2	4 / 5
48.0	5.0	300	12	4 / 5

SiC464, SiC474 EVB TYPICAL PRE-DEFINED OPERATING CONFIGURATIONS				
V_{IN} (V)	V_{OUT} (V)	f_{sw} (kHz)	L (µH)	MAXIMUM I_{OUT} (A) SiC464 / SiC474
48.0	3.3	300	15	2 / 3
48.0	5.0	300	22	2 / 3

CONNECTION AND SIGNAL / TEST POINTS

Power Terminals (J4)

V_{IN}, GND (J4, pin 1 and pin 2): (see Fig. 1)

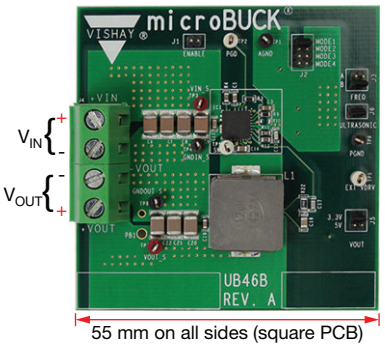


Fig. 1 - PCB Showing Power Terminal Connections

Connect to a voltage source: 4.5 V to 50 V.

V_{OUT}, GND (J4, pin 3 and pin 4): (see Fig. 1)

Connect to a load that draws no more than:
SiC463 - 4 A, SiC464 - 2 A
SiC473 - 5 A, SiC474 - 3 A

The output voltage is selectable on J5

Warning

The output capacitors are rated to 25 V. Should a higher output voltage be required, the output capacitors must be changed to ones with an appropriate higher voltage rating.

SELECTION JUMPERS

Operation Mode Select Using J2 and J6

J2 allows the user to select modes of power saving and whether using an internal LDO regulator or an external power supply as V_{DRV} for operation.

J6 allows the user to further select the ultrasonic mode of power saving. In ultrasonic mode the minimum frequency of operation is 20 kHz, above the audible range. When not in ultrasonic mode the frequency can drop below 20 kHz.

The table below lists all modes of operation and their related jumper setup

OPERATION MODES					
MODE	POWER SAFE MODE	V_{DRV} SUPPLY	J2 SETUP	ULTRASONIC ENABLED	J6 SETUP
1	Enabled	Internal LDO	Pin 1 to 2 shorted	Yes	Shorted
				No	Open
2	Disabled	Internal LDO	Pin 3 to 4 shorted	n/a	Open
3	Disabled	External supply	Pin 5 to 6 shorted	n/a	Open
4	Enabled	External supply	Pin 7 to 8 shorted	Yes	Shorted
				No	Open

External V_{DRV} Supply

5 V (TP5), GND (TP6): this is the terminal that enables the user to use an external 5 V_{DC} supply as MOSFET gate driver supply when mode 3 or mode 4 in table “Operation Modes” is selected. This should only be used in modes 3 and mode 4.

Enable

J1 is a 2 pin header crossing EN pin to ground.

The EN pin has an internal high impedance pull down resistor and requires an DC voltage higher than 1.35 V to enable chip operation. Shorting J1 with a jumper will disable the chip operation.

Output Voltage V_{OUT} Setting

J5 allows the user to set 3.3 V or 5.0 V output voltage V_{OUT}. J5 is a 2 x 2 eight pin header and the table below lists the available voltage setting and related jumper setup. The user can use equation in datasheets to calculate required resistance for a designated output voltage.

OUTPUT VOLTAGE SETTING		
V_{OUT} DESIRED (V)	J5 SETUP	RESISTANCE BETWEEN V_{OUT} AND FB PIN (kΩ)
3.3	Pin 1 to 2 shorted	31.6
5.0	Pin 3 to 4 shorted	52.3

Switching Frequency f_{sw} Setting

J3 allows the user to achieve 300 kHz switching frequency after the users set up output voltage following table “Output Voltage Setting”. J3 is a 2 x 2 four pin header and it generates logic level of input pins of U1 (DG2034, multiplexers). Table “Switching Frequency Setting” lists the related logic level of U1 matching different output voltages in table “Output Voltage Setting” and related J3 jumper setup. The user can use equation in datasheet to calculate required resistance to achieve a desired switching frequency with a designated output voltage.

SWITCHING FREQUENCY SETTING

SWITCHING FREQUENCY DESIRED (kHz)	V_{OUT} (V) [1]	U1 INPUT LOGIC	J3 JUMPER SETUP	RESISTANCE BETWEEN f_{sw} AND GND (kΩ)
300	3.3	2‘b01	Pin 1 to 2 shorted	57.6
	5.0	2‘b10	Pin 3 to 4 shorted	88.7

Note

(1) V_{OUT} set in table “Output Voltage Setting”

SIGNALS AND TEST LEADS

Input Voltage Sense

V_{IN_SENSE} (TP3), GND_{IN_SENSE} (TP4): this allows the user to measure the voltage directly at the input of the regulator bypassing any losses generated by connections to the board. These test points can also be as a remote sense port of a power source with remote sense capability.

Output Voltage Sense

V_{OUT_SENSE} (TP7), GND_{OUT_SENSE} (TP8): this allows the user to measure the output voltage directly at the sense point of the regulator bypassing any losses generated by connections to the board. These test points can also be as a remote sense port of an external load with remote sense capability.

Power Good Indicator

P_{GOOD}: is an open drain output and is pulled up with a 102 kΩ resistor, R3, to V_{DD} (5 V). When FB or V_{OUT} are within -10 % to +20 % of the set voltage this pin will go HI to indicate the output is okay.

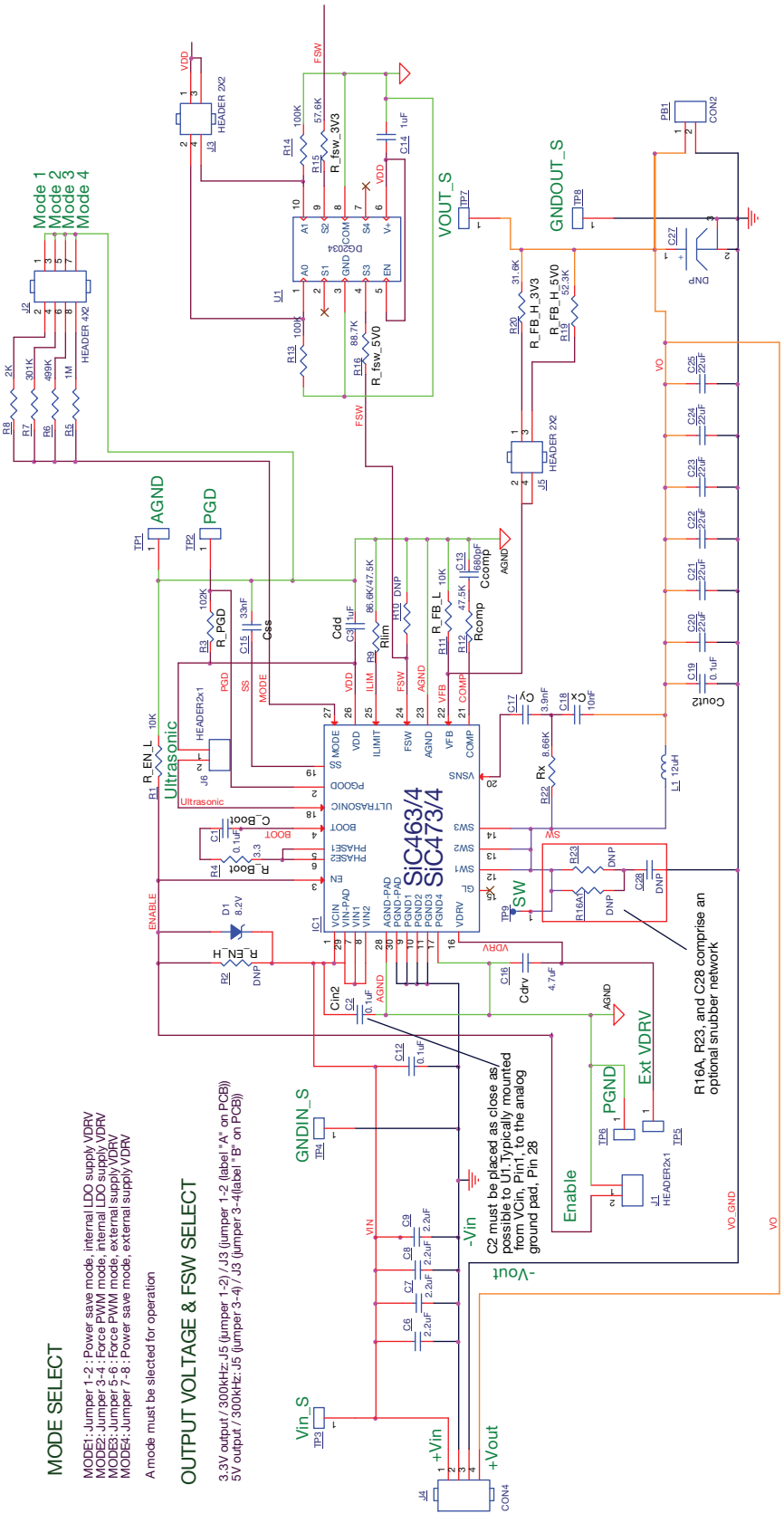
Power Up Procedure

Before turning on the reference board, the user needs to select one of the four modes by shorting one jumper (see section on mode selection). If mode 3 or mode 4 is selected, make sure V_{DRV} pin is supplied by external 5 V. There is no specific power sequence requirement to power up the board.

Snubber Circuit

Snubber may be used when the user desire to decrease the peak voltage of switching node SW during turn on of the high side switch. There are place holders on the reference board, R16A1, R23, and C28, for the snubber.

SCHEMATIC FOR SiC463, SiC464, SiC473, AND SiC474



PCB LAYOUT FOR SiC463, SiC464, SiC473, AND SiC474

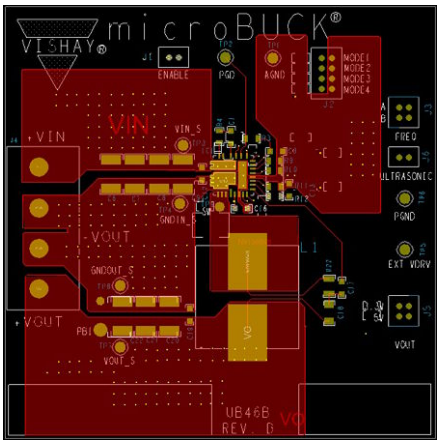


Fig. 2 - Top Layer

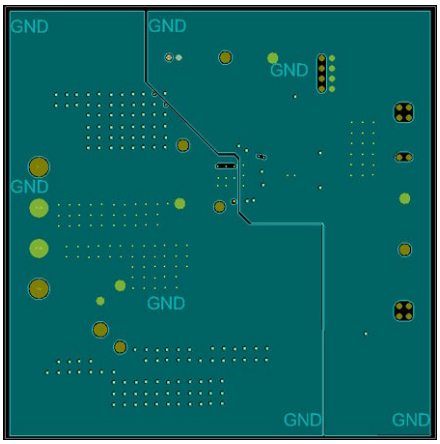


Fig. 4 - Inner Layer 2

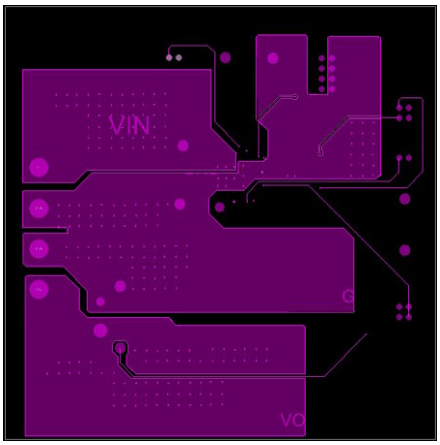


Fig. 3 - Inner Layer 3

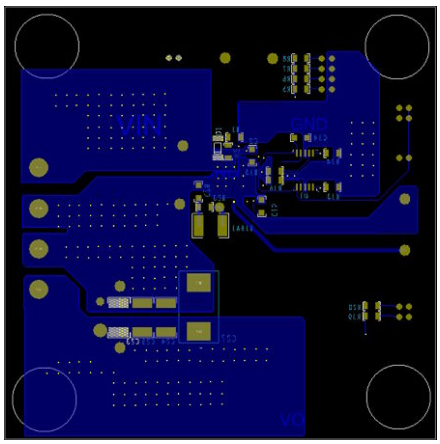


Fig. 5 - Bottom Layer

BILL OF MATERIAL REPORT FOR SiC463, SiC464, SiC473, AND SiC474						
SYM_NAME	BOM FOR SiC463	BOM FOR SiC464	BOM FOR SiC473	BOM FOR SiC474	QTY	REFDES
1210	DNP	DNP	DNP	DNP	1	R16A1
0603	0.1 µF ±10 % 50 V X7R 0603	0.1 µF ±10 % 50 V X7R 0603	0.1 µF ± 10 % 50 V X7R 0603	0.1 µF ± 10 % 50 V X7R 0603	1	C1; C19
0603	0.1 µF ±10 % 100 V X7R 0603	0.1 µF ± 10 % 100 V X7R 0603	0.1 µF ± 10 % 100 V X7R 0603	0.1 µF ± 10 % 100 V X7R 0603	2	C2; C12;
0603	1 µF ±10 % 25 V X7R 0603	1 µF ± 10 % 25 V X7R 0603	1 µF ± 10 % 25 V X7R 0603	1 µF ± 10 % 25 V X7R 0603	2	C3, C14
0603	680 pF ± 5 % 50 V C0G/NP0 0603	680 pF ± 5% 50 V C0G/NP0 0603	680 pF ± 5 % 50 V C0G/NP0 0603	680 pF ± 5 % 50 V C0G/NP0 0603	1	C13
0603	33 nF ±10 % 25 V X7R 0603	33 nF ± 10 % 25 V X7R 0603	33 nF ± 10 % 25 V X7R 0603	33 nF ± 10 % 25 V X7R 0603	1	C15
0603	4.7 µF ± 10 % 10 V X7S 0603	4.7 µF ± 10 % 10 V X7S 0603	4.7 µF ± 10 % 10 V X7S 0603	4.7 µF ± 10 % 10 V X7S 0603	1	C16
0603	3.9 nF ± 5 % 50 V C0G/NP0 0603	3.9 nF ± 5 % 50 V C0G/NP0 0603	3.9 nF ± 5 % 50 V C0G/NP0 0603	3.9 nF ± 5 % 50 V C0G/NP0 0603	1	C17
0603	DNP	DNP	DNP	DNP	1	C28
0805	10 nF ± 5 % 50 V C0G/NP0 0805	10 nF ± 5 % 50 V C0G/NP0 0805	10 nF ± 5 % 50 V C0G/NP0 0805	10 nF ± 5 % 50 V C0G/NP0 0805	1	C18
1210	2.2 µF ± 10 % 100 V X7R 1210	2.2 µF ± 10 % 100 V X7R 1210	2.2 µF ± 10 % 100 V X7R 1210	2.2 µF ± 10 % 100 V X7R 1210	4	C6; C7; C8; C9
1210	22 µF ± 10 % 25 V X7R 1210	22 µF ± 10 % 25 V X7R 1210	22 µF ± 10 % 25 V X7R 1210	22 µF ± 10 % 25 V X7R 1210	6	C20; C21; C22; C23; C24; C25
	DNP	DNP	DNP	DNP	0	C27
ED120-4DS2	CON4	CON4	CON4	CON4	1	J4
	IHLP5050FDER120M51 12 µH, 20 %, 19 mΩ DCR, 10.6 A I_{RMS}, 6.9 A $I_{SAT\,1}$ at 25 °C (20% roll off)	IHLP5050FDER220M51 22 µH, 20 %, 31.3 mΩ DCR, 8.3 A I_{RMS}, 5.5 A $I_{SAT\,1}$ at 25 °C (20% roll off)	IHLP5050FDER120M51 12 µH, 20 %, 19 mΩ DCR, 10.6 A I_{RMS}, 6.9 A $I_{SAT\,1}$ at 25 °C (20% roll off)	IHLP5050FDER220M51 22 µH, 20 %, 31.3 mΩ DCR, 8.3 A I_{RMS}, 5.5 A $I_{SAT\,1}$ at 25 °C (20% roll off)	1	L1 (recommended for V_{OUT} = 5.0 V)
	IHLP5050FDER8R2M01 8.2 µH, 20 %, 14.5 mΩ DCR, 10.5 A I_{RMS}, 16 A $I_{SAT\,1}$ at 25 °C (20% roll off)	IHLP5050FDER150M51 15 µH, 20 %, 24 mΩ DCR, 8.7 A I_{RMS}, 6.8 A $I_{SAT\,1}$ at 25 °C (20% roll off)	IHLP5050FDER8R2M01 8.2 µH, 20 %, 14.5 mΩ DCR, 10.5 A I_{RMS}, 16 A $I_{SAT\,1}$ at 25 °C (20% roll off)	IHLP5050FDER150M51 15 µH, 20 %, 24 mΩ DCR, 8.7 A I_{RMS}, 6.8 A $I_{SAT\,1}$ at 25 °C (20% roll off)	1	L1 (DNP) (recommended for V_{OUT} = 3.3 V)
MINIJUMPER2	HEADER 2 x 1	HEADER 2 x 1	HEADER 2 x 1	HEADER 2 x 1	2	J1, J6
MINIJUMPER2X2	HEADER 2 x 2	HEADER 2 x 2	HEADER 2 x 2	HEADER 2 x 2	2	J3; J5
MINIJUMPER2X4	HEADER 4 x 2	HEADER 4 x 2	HEADER 4 x 2	HEADER 4 x 2	1	J2
MSOP10	DG2034	DG2034	DG2034	DG2034	1	U1
0603	10 kΩ ± 1 %	10 kΩ ± 1 %	10 kΩ ± 1 %	10 kΩ ± 1 %	2	R1; R11
0603	DNP		DNP		3	R2; R10; R23
0603	102 kΩ ± 1 %	102 kΩ ± 1 %	102 kΩ ± 1 %	102 kΩ ± 1 %	1	R3
0603	3.3 Ω ± 1 %	3.3 Ω ± 1 %	3.3 Ω ± 1 %	3.3 Ω ± 1 %	1	R4
0603	1 MΩ ± 1%	1 MΩ ± 1%	1 MΩ ± 1%	1 MΩ ± 1%	1	R5
0603	499 kΩ ± 1%	499 kΩ ± 1%	499 kΩ ± 1%	499 kΩ ± 1%	1	R6
0603	301 kΩ ± 1%	301 kΩ ± 1%	301 kΩ ± 1%	301 kΩ ± 1%	1	R7
0603	2 kΩ ± 1%	2 kΩ ± 1%	2 kΩ ± 1%	2 kΩ ± 1%	1	R8
0603	47 kΩ	78.7 kΩ	47 kΩ	78.7 kΩ	1	R9
0603	47.5 kΩ ± 1%	47.5 kΩ ± 1%	47.5 kΩ ± 1%	47.5 kΩ ± 1%	1	R12
0603	100 kΩ ± 1%	100 kΩ ± 1%	100 kΩ ± 1%	100 kΩ ± 1%	2	R13; R14
0603	57.6 kΩ ± 1%	57.6 kΩ ± 1%	57.6 kΩ ± 1%	57.6 kΩ ± 1%	1	R15

BILL OF MATERIAL REPORT FOR SiC463, SiC464, SiC473, AND SiC474						
SYM_NAME	**BOM FOR SiC463**	**BOM FOR SiC464**	**BOM FOR SiC473**	**BOM FOR SiC474**	**QTY**	**REFDES**
0603	88.7 kΩ ± 1%	88.7 kΩ ± 1%	88.7 kΩ ± 1%	88.7 kΩ ± 1%	1	R16
0603	52.3 kΩ ± 1%	52.3 kΩ ± 1%	52.3 kΩ ± 1%	52.3 kΩ ± 1%	1	R19
0603	31.6 kΩ ± 1%	31.6 kΩ ± 1%	31.6 kΩ ± 1%	31.6 kΩ ± 1%	1	R20
0805	8.66 kΩ ± 1%	8.66 kΩ ± 1%	8.66 kΩ ± 1%	8.66 kΩ ± 1%	1	R22
	SiC463	**SiC464**	**SiC473**	**SiC474**	1	IC1
SOD323	8.2 V	8.2 V	8.2 V	8.2 V	1	D1
	Test point, red	Test point, red	Test point, red	Test point, red	2	TP3, TP7
	Test point, black	Test point, black	Test point, black	Test point, black	4	TP4, TP8, TP1, TP6
	Test point, white	Test point, white	Test point, white	Test point, white	2	TP9, TP5
JUMPER					5	TP2
	UB46**B**	UB46**B**	UB46**B**	UB46**B**	1	OFF BOARD x **5**