Power MOSFET Avalanche Design Guidelines

TABLE OF CONTENTS

The purpose of this note is to better understand and utilize power MOSFETs, it is important to explore the theory behind avalanche breakdown and to understand the design and rating of rugged MOSFETs. Several different avalanche ratings are explained and their usefulness and limitations in design is considered.

APPLICATION NOTE

Power MOSFET Avalanche Design Guidelines

TABLE OF FIGURES

Power MOSFET Avalanche Design Guidelines

INTRODUCTION

Overview

To better understand and utilize power MOSFETs, it is important to explore the theory behind avalanche breakdown and to understand the design and rating of rugged MOSFETs. Several different avalanche ratings are explained and their usefulness and limitations in design is considered.

Avalanche Mode Defined

All semiconductor devices are rated for a certain max. reverse voltage (BV_{DSS} for power MOSFETs). Operation above this threshold will cause high electric fields in reversed biased p-n junctions. Due to impact ionization, the high electric fields create electron-hole pairs that undergo a multiplication effect leading to increased current. The reverse current flow through the device causes high power dissipation, associated temperature rise, and potential device destruction.

Avalanche Occurrences In Industry Applications

Flyback Converter Circuit

Some designers do not allow for avalanche operation; instead, a voltage derating is maintained between rated BV_{DSS} and V_{DD} (typically 90 % or less). In such instances, however, it is not uncommon that greater than planned for voltage spikes can occur, so even the best designs may encounter an infrequent avalanche event. One such example, a flyback converter, is shown in figures 1 to 3.

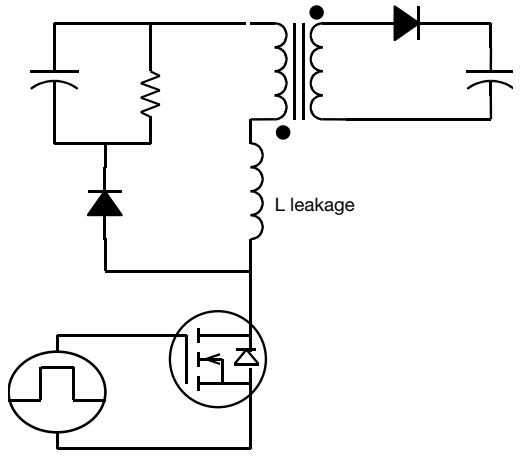

Fig. 1 - Flyback Converter Circuit

During MOSFET operation of the flyback converter, energy is stored in the leakage inductor. If the inductor is not properly clamped, during MOSFET turnoff the leakage inductance discharges through the primary switch and may cause avalanche operation as shown in the V_{DS}, I_D, and V_{GS} vs. time waveforms in figures 2 and 3.

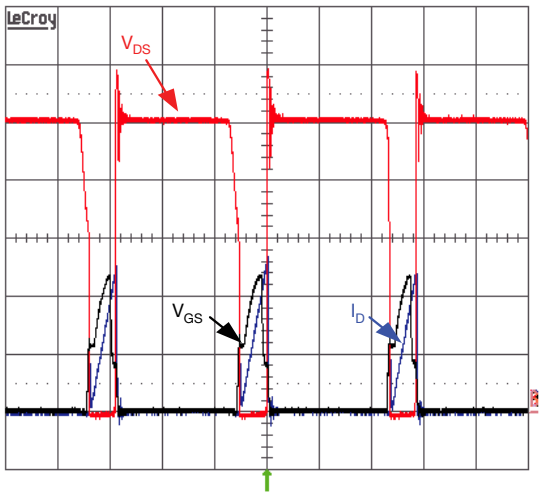

Fig. 2 - Flyback Converter Switch Under Avalanche Waveform

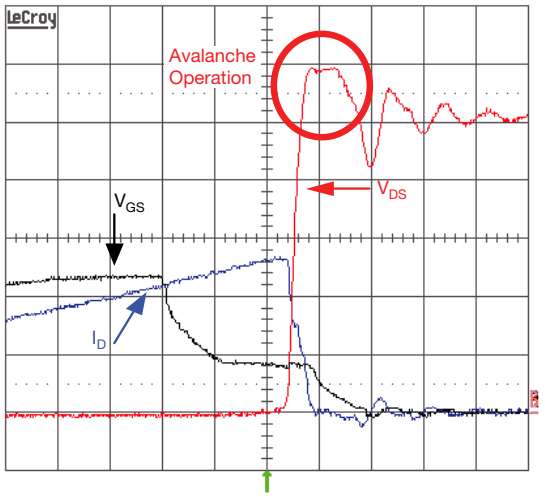

Fig. 3 - Flyback Converter Switch Under Avalanche Waveform (Detail)

Note

- **Red (V_{DS}), Blue (I_D), Black (V_{GS})**

In this application, built in avalanche capability is an additional power MOSFET feature and safeguards against unexpected voltage over-stresses that may occur at the limits of circuit operation.

APPLICATION NOTE

Power MOSFET Avalanche Design Guidelines

AVALANCHE FAILURE MODE

Some power semiconductor devices are designed to withstand a certain amount of avalanche current for a limited time and can, therefore, be avalanche rated. Others will fail very quickly after the onset of avalanche. The difference in performance stems from particular device physics, design, and manufacturing.

Power MOSFET Device Physics

All semiconductor devices contain parasitic components intrinsic to the physical design of the device. In power MOSFETs, these components include capacitors due to displaced charge in the junction between p and n regions, resistors associated with material resistivity, a body diode formed where the p+ body diffusion is made into the n- epi-layer, and an NPN (bi-polar junction transistor henceforth called BJT) sequence (BJT) formed where the n+ source contact is diffused. See figure 4 for power MOSFET cross section that incorporates the parasitic components listed above and figure 5 for a complete circuit model of the device.

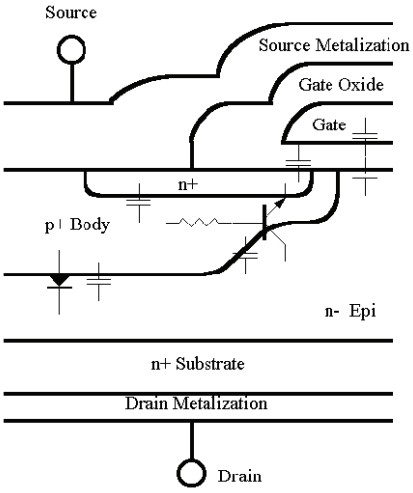

Fig. 4 - Power MOSFET Cross Section

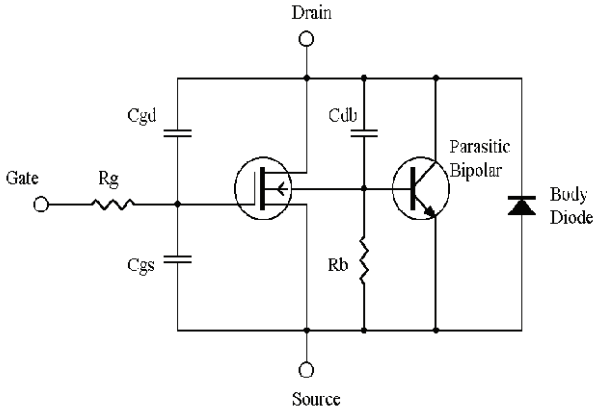

Fig. 5 - Power MOSFET Circuit Model

In avalanche, the p-n junction acting as a diode no longer blocks voltage. With higher applied voltage a critical field is reached where impact ionization tends to infinity and carrier concentration increases due to avalanche multiplication. Due to the radial field component, the electric field inside the device is most intense at the point where the junction bends. This strong electric field causes maximum current flow in close proximity to the parasitic BJT, as depicted in figure 6 below. The power dissipation increases temperature, thus increasing R_B, since silicon resistivity increases with temperature. From Ohm's Law we know that increasing resistance at constant current creates an increasing voltage drop across the resistor. When the voltage drop is sufficient to forward bias the parasitic BJT, it will turn on with potentially catastrophic results, as control of the switch is lost.

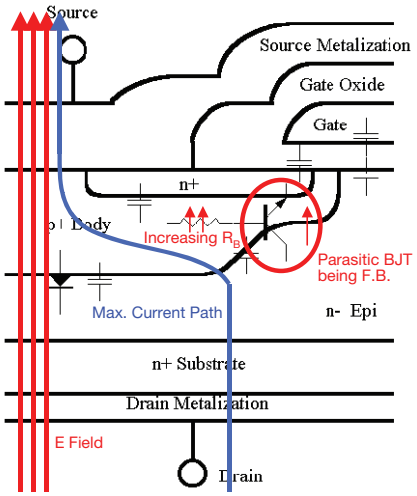

Fig. 6 - Power MOSFET Cross Section Under Avalanche

Typical modern power MOSFETs have millions of identical trenches, cells or many strips in parallel to form one device, as shown in figure 7. For robust designs, then, avalanche current must be shared among many cells/strips evenly. Failure will then occur randomly in a single cell, at a high temperature. In weak designs, the voltage required to reach breakdown electric field is lower for one device region (group of cells) than for others, so critical temperature will be reached more easily causing the device to fail in one specific area.

APPLICATION NOTE

Power MOSFET Avalanche Design Guidelines

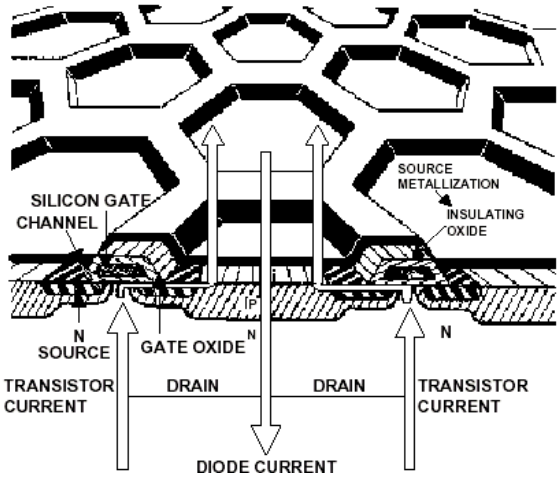

Fig. 7 - Basic Power MOSFET Cell Structure

Rugged MOSFETs

First introduced in the middle 1980's, avalanche rugged MOSFETs are designed to avoid turning on the parasitic BJT until very high temperature and/or very high avalanche current occur. This is achieved by:

- Reducing the p+ region resistance with higher doping diffusion
- Optimizing cell/line layout to minimize the "length" of R_B

The net effect is a reduction of R_B, and thus the voltage drop necessary to forward bias the parasitic BJT will occur at higher current and temperature.

Avalanche rugged MOSFETs are designed to contain no single consistently weak spot, so avalanche occurs uniformly across the device surface until failure occurs randomly in the active area. Utilizing the parallel design of cells, avalanche current is shared among many cells and failure will occur at higher current than for designs with a single weak spot. A power MOSFET which is well designed for ruggedness will only fail when the temperature substantially exceeds rated $T_{J\ (max.)}$.

An analysis of various MOSFET devices tested to destruction indicates that failure spots occur randomly in the active area. Some samples are shown in the figure 8:

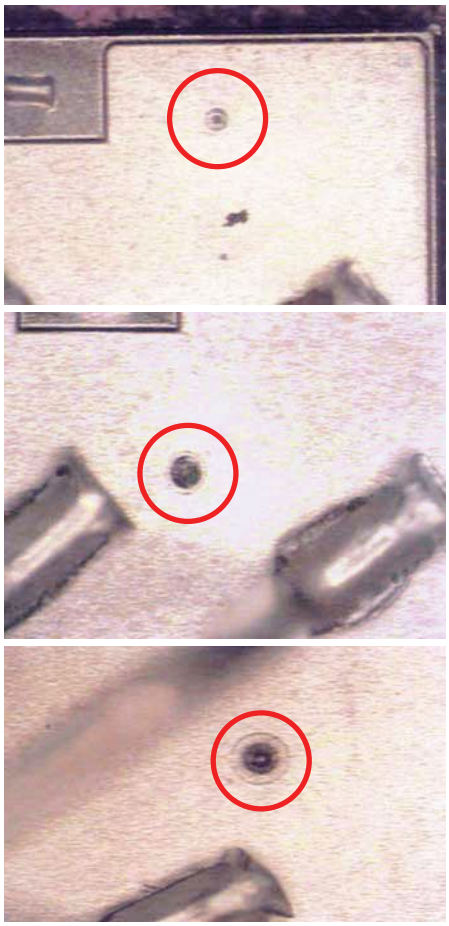

Fig. 8 - Power MOSFET Random Device Failure Spots

The risk of manufacturing process or fabrication induced "weak cell" parts is always present. The SEM cross-section micrograph on the top shows one such example. The source metal contacts the n+ layer at the near surface, but not the p+ layer. As a result the BJT base is floating and easily triggerable. An example of a good contact is shown on the bottom. The source metal contacts and shorts the n+ layer to the p+ layer thus supressing the parasitic BJT operation.

APPLICATION NOTE

Power MOSFET Avalanche Design Guidelines

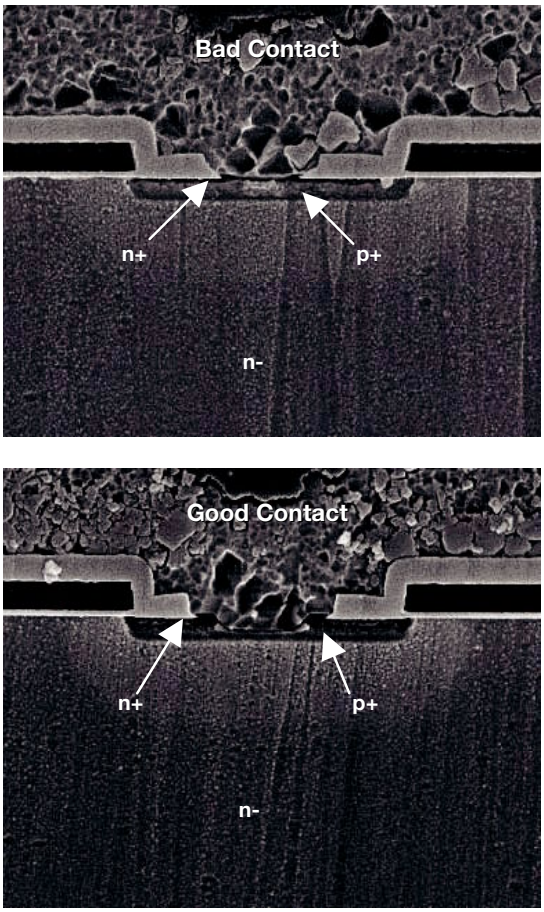

Fig. 9 - Good Source Contact vs. Bad Source Contact Illustration

Parts with weak cells such as are shown on the top of figure 9 can be removed from the population by 100 % avalanche (E_{AS}) stress testing during production.

A "three legged" approach is used during design:

1. Statistically significant samples of prospective designs are tested to failure at test conditions chosen to reach extremes in temperature and current stress. Representative parts from DOE elements are tested to assure uniform avalanche failure across expected variation of critical process steps.
2. Each design is tested to failure across temperature and inductor (time in avalanche) to assure that failure extrapolates to zero at a temperature well in excess of $T_{J\ (max.)}$. (See sample figure 10 of "I_{AS} at failure vs. T_{start}" below.)
3. A sample of final design parts are stressed with repetitive avalanche pulses of such a value to raise junction temperature to $T_{J\ (max.)}$.

This "three legged" solution helps assure that designs are rugged and can be avalanche rated.

The following factors are used to provide rugged avalanche MOSFETs:

- Improved device design:
  - To mute the parasitic BJT by reducing R_B
  - To eliminate the effect of weaker cells in particular positions of the layout (i.e. cells along device termination, gate bussing, etc.)
- Improved manufacturing process:
  - To guarantee more uniform cells
  - To reduce incomplete or malformed cell occurrences
- Improved device characterization:
  - To assure devices fail uniformly across wide range of I_D, temperature
  - To assure device fails at very high (extrapolated) temperature
  - To assure device is capable of surviving multiple avalanche cycles at the thermal limit
- 100 % avalanche stress testing

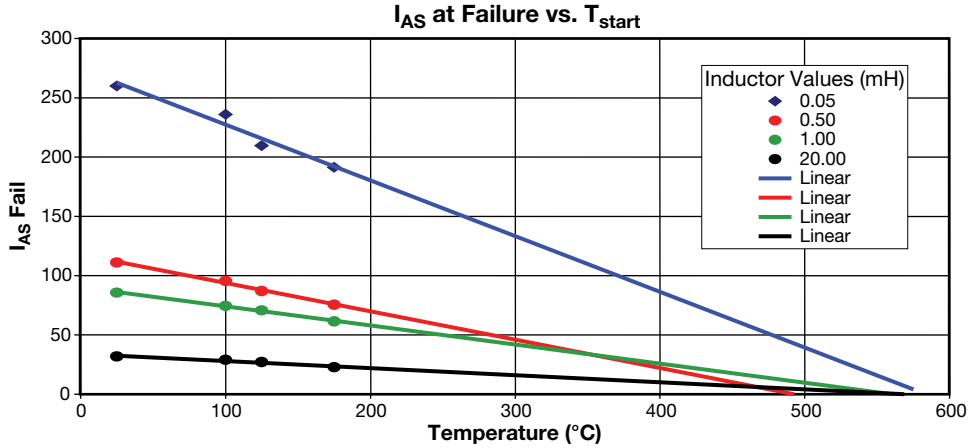

Fig. 10 - I_{AS} at Failure vs. Test Temperature

APPLICATION NOTE

Power MOSFET Avalanche Design Guidelines

AVALANCHE TESTING DETAILS

Vishay performs avalanche stress testing on its power semiconductor devices to assure conformance of new designs with avalanche rating, to validate parts for ruggedness, and to screen production for weak devices.

Single Pulse Unclamped Inductive Switching

A single pulse unclamped inductive switching test circuit for avalanche testing that is shown below in figures 11 and 12. This circuit is still referenced in older "legacy" product datasheets.

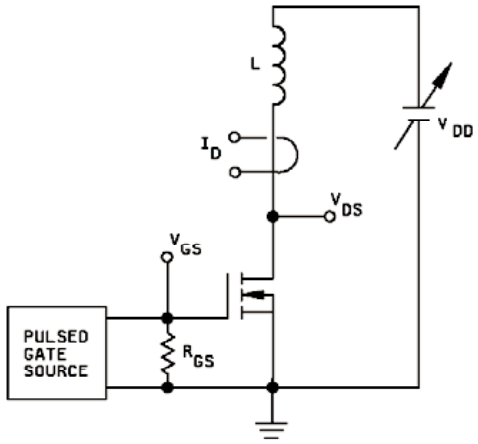

Fig. 11 - Single Pulse Unclamped Inductive Switching Test Circuit

From the figure 11 schematic we can calculate the single pulse avalanche energy (E_{AS}) as:

$$E_{AS} = \frac{L \times (I_{AS})^2}{2} \times \frac{V_{DS}}{V_{DS} - V_{DD}} \quad (1)$$

The measured energy values depend on the avalanche breakdown voltage, which tends to vary during the discharge period due to the temperature increase. Also note that for low voltage devices V_{DS} - V_{DD} may become quite small, limiting the use of this circuit since it introduces high-test error.

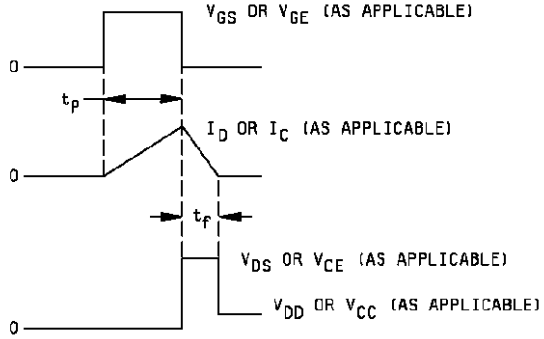

Fig. 12 - Single Pulse Unclamped Inductive Switching Test Circuit Output Waveforms

Decoupled V_{DD} Voltage Source

To surpass the limitations of the single pulse unclamped inductive switching test circuit, the decoupled V_{DD} voltage source illustrated in figures 13 and 14 is used.

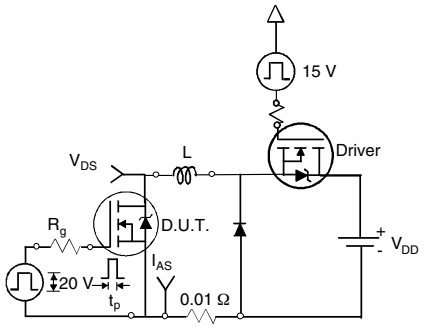

Fig. 13 - Decoupled V_{DD} Voltage Source Test Circuit Model

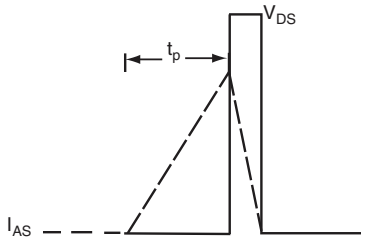

Fig. 14 - Decoupled V_{DD} Voltage Source Test Circuit Waveforms

Here a driver FET and recirculation diode are added so that the voltage drop across the inductor during avalanche is equal to the avalanche voltage. With this circuit (neglecting the angular E_{SR} in the inductor) the energy can be simply calculated as:

$$E_{AS} = \frac{1}{2} L \times (I_{AS})^2 \quad (2)$$

A better and more accurate reading of the avalanche energy can be obtained by measuring instantaneous voltage and current in the device and integrating as described in the following equation:

$$E_{AS} = \int_{t_1}^{t_2} V_{(AV)DSS}(t) \times I_{AS}(t) \times dt \quad (3)$$

For further reference, figures 15 and 16, depict ideal and actual avalanche waveforms, respectively.

APPLICATION NOTE

Power MOSFET Avalanche Design Guidelines

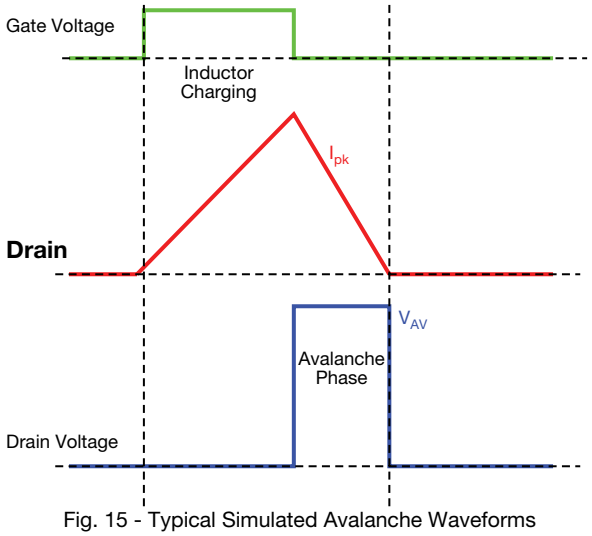

Fig. 15 - Typical Simulated Avalanche Waveforms

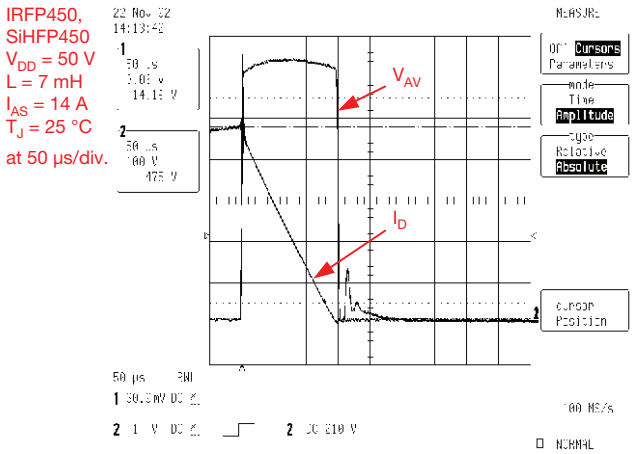

Fig. 16 - IRFP450, SiHFP450 (500 V Rated) Device Avalanche Waveforms

Note that the peak avalanche voltage V_{AV} can be approximated as 1.3 times the device rating, or 650 V.

AVALANCHE RATING

Generally, there are three approaches to avalanche rating devices:

1. **Thermal Limit Approach:** The device is rated to the value(s) of energy, E_{AS}, that causes an increase in junction temperature up to $T_{J\ (max.)}$. E_{AS} avalanche rated MOSFETs are rated in this manner.
2. **Statistical Approach:** Devices are tested up to the failure point. The rating is given using statistical tools (e.g., average (E_{AS}) - 6 σ) applied to the failure distribution. Some parts are rated this way and indicated as E_{AS} (tested), generally in addition to the thermally limited rating. However, some MOSFET suppliers provide only this rating on their datasheets.
3. No rating at all.
   While the first two approaches provide a value for avalanche energy, the designer must take care to know the important differences that are outlined below.

Further note that $V_{(BR)DSS}$ and V_{AV} are used interchangeably in this text.

E_{AS} THERMAL LIMIT APPROACH

Single Pulse

The single pulse avalanche rating (E_{AS}) is based on the assumption that the device is rugged enough to sustain avalanche operation under a wide set of conditions subjection only to not exceeding the maximum allowed junction temperature. Typically, the avalanche rating on the datasheet is the value of the energy that increases the junction temperature from 25 °C to $T_{J\ (max.)}$, assuming a constant case temperature of 25 °C and assuming a specified value of I_D (usually set at 60 % of I_D (25 °C).

For example, consider the 500 V/32 A device as excerpted from the datasheet below,

V_{DSS}	$R_{DS(on)}$typ.	I_D
500V	0.135Ω	32A

P_D@T_C = 25°C	Power Dissipation	460	W

Avalanche Characteristics

② Starting T_J = 25°C, L = 0.87mH, R_G = 25Ω, I_{AS} = 32A.

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	——	450	mJ
I_{AR}	Avalanche Current①	——	32	A
E_{AR}	Repetitive Avalanche Energy①	——	46	mJ

① Repetitive rating; pulse width limited by max. junction temperature.

T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Fig. 17 - IRFP32N50K, SiHFP32N50K Datasheet Excerptions

Power MOSFET Avalanche Design Guidelines

with the following initial conditions:

- Single pulse avalanche current: $I_{AS} = I_D = 32$ A
- Starting temperature: $T_{start} = 25$ °C
- Inductor value: L = 0.87 mH

To calculate the temperature increase due to the avalanche power dissipation we utilize a thermal model with Ohm's Law equivalence. The resulting equation follows:

$$\Delta T = Z_{TH} \times P_{AV} \quad (4)$$

The average power dissipated during avalanche can be calculated as

$$P_{AV} = \frac{1}{2}\left(\frac{V_{AV} \times I_{AS} \times t_{AV}}{t_{AV}}\right) = 0.5 \times 650\ V \times 32\ A = 10\ kW \quad (5)$$

Avalanche voltage can be estimated as

$$V_{AV} \cong 1.3 \times BV_{DSS} = 1.3 \times 500\ V = 650\ V \quad (6)$$

Now from equation 2 we can calculate

$$E_{AS} = \frac{1}{2} L \times (I_{AS})^2 = 0.5 \times 0.87\ mH \times 32^2 = 445\ mJ$$

which agrees with the datasheet value within rounding of the least significant digit.

The duration of the avalanche power pulse can be calculated, assuming the inductor is discharging with a constant voltage applied to it, as

$$t_{AV} \cong L \times \frac{I_{pk}}{V_{AV}} = 0.87\ mH \times \frac{32\ A}{650\ V} \cong 43\ \mu s \quad (7)$$

The thermal impedance (Z_{TH}) for this pulsewidth can be read from the transient thermal impedance plot provided with the datasheet, as shown in figure 18.

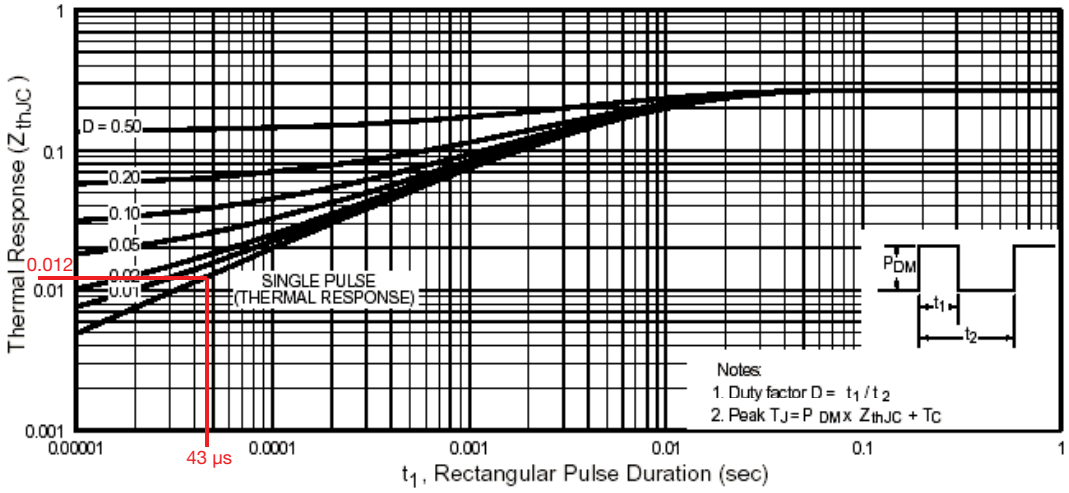

Fig. 18 - Transient Thermal Impedance Plot, Junction-to-Case

The temperature increase due to avalanche and the final junction temperature can therefore be calculated using equation 4

$$\Delta T = Z_{TH} \times P_{AV} = 0.012 \times 10\ kW = 120\ °C$$
$$T_J = T_{start} + \Delta T = 145\ °C \leq T_{J\,(max.)} = 150\ °C \quad (8)$$

showing that the datasheet rating is consistent with the calculated $T_{J\,(max.)}$ within minor error due to reading Z_{TH} from figure 18.

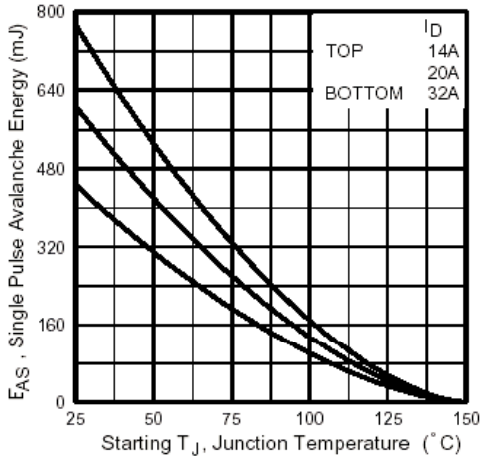

Fig. 19 - Maximum Avalanche Energy vs. Temperature For Various Drain Currents

APPLICATION NOTE

Power MOSFET Avalanche Design Guidelines

Figure 19 is included in datasheets for E_{AS} rated parts and shows many values of E_{AS} for varying starting T_J and I_D. Each point along the curves shown represents the energy necessary to raise the temperature to $T_{J\ (max.)}$.

Note that this curve belies the myth of trying to compare datasheet table E_{AS} values : by varying current and/or temperature the E_{AS} value can vary by a range of 800 x! Specifying E_{AS} at lower I_D values results in higher E_{AS} even though the device stress (T_J) is the same.

Repetitive Pulse

Historically, the repetitive pulse avalanche energy (E_{AR}) was rated at 1/10 000 of P_D (25 °C). This practice is now supplanted on newer products by an explicit rating of avalanche operation up to the $T_{J\ (max.)}$ condition.

Datasheets utilizing this newer rating also include:

- E_{AS}: the single pulse rating
- Z_{TH} graph: Z_{TH} vs. time for various duty cycles (example in figure 18 preceded by discussion)
- E_{AS} graph: E_{AS} vs. T_{start} for various I_D (example in figure 19 followed by discussion)
- E_{AR} graph: E_{AR} vs. T_{start} for various duty cycles, single I_D (example and discussion to follows)
- I_{AR} graph: Typical avalanche current vs. pulsewidth for various duty cycles (example and discussion to follow below)

The E_{AR} graph shows the avalanche energy necessary to raise the junction temperature from the starting temperature to $T_{J\ (max.)}$ for various duty cycles, at a given current. A sample E_{AR} graph is given in figure 20. The top curve represents single pulse behavior at 125 A, while the bottom curve represents repetitive pulse operation at 125 A, 10 % duty cycle. In repetitive pulse operation, the junction temperature does not have sufficient time between pulses to return to the ambient level. The larger the duty cycle, the higher the junction temperature will be when the next pulse arrives. Therefore, with increasing duty cycle, the avalanche energy required to raise the junction temperature to $T_{J\ (max.)}$ will be lower.

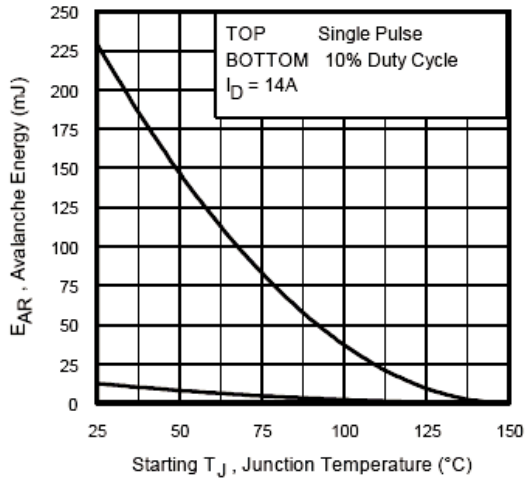

Fig. 20 - E_{AR} vs. T_{start} For Various Duty Cycles, Single I_D

The I_{AR} graph (see figure 21) shows how the avalanche current varies with the avalanche pulsewidth for various duty cycles, with a “budgeted” increase in junction temperature due to avalanche losses assumed at (ΔT) = 25 °C. An effect similar to that in the E_{AR} graph occurs. In repetitive pulse operation, the junction temperature does not have sufficient time to decrease to the ambient temperature between pulses. As a result, the starting temperature for subsequent pulses will be higher than the ambient temperature. Therefore, a smaller amount of avalanche energy, corresponding to smaller avalanche current, will raise the junction temperature to $T_{J\ (max.)}$ for subsequent pulses. So for increasing duty cycles, the avalanche current required to raise the junction temperature by 25 °C will decrease.

A detailed specific example now follows to illustrate how to design for repetitive avalanche operation for the 40 V/14 A MOSFET (see figure 22).

APPLICATION NOTE

Power MOSFET Avalanche Design Guidelines

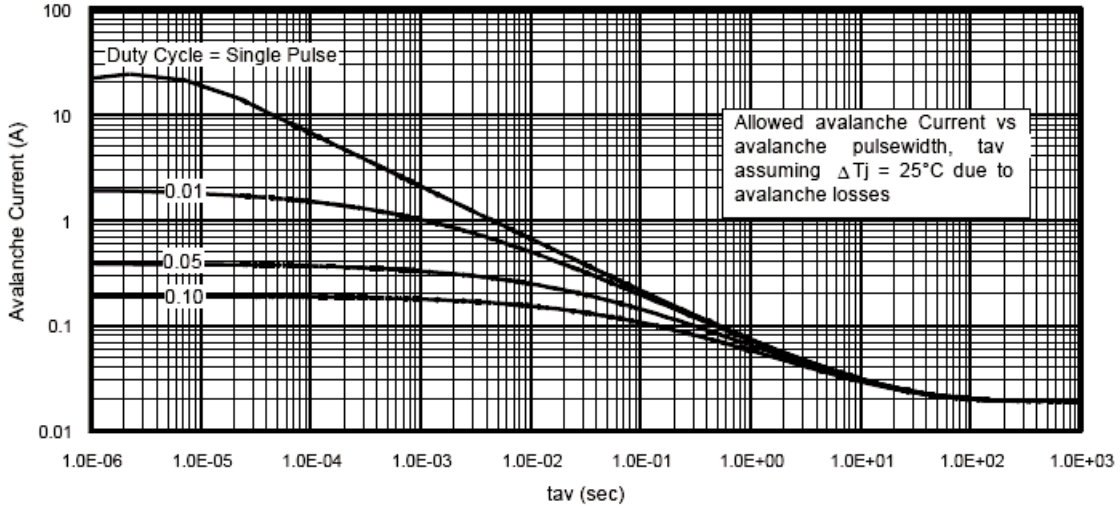

Fig. 21 - Typical Avalanche Current vs. Pulsewidth For Various Duty Cycles

V_{DSS}	$R_{DS(on)}$ max (mΩ)	I_D
40V	10@V_{GS} = 7.0V	14A

Absolute Maximum Ratings

	Parameter	Max.	Units
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	---	20	°C/W
$R_{\theta JA}$	Junction-to-Ambient ③	---	50	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	10	mΩ	V_{GS} = 7.0V, I_D = 14A ②

Fig. 22 - Specification of 40 V/14 A MOSFET Datasheet Excerptions

The initial conditions are:

- Ambient temperature: T_A = 120 °C
- Solenoid inductance: L = 5 mH
- Solenoid resistance: R_L = 15 Ω
- Pulse frequency: f = 125 Hz
- Supply voltage: V_{DD} = 14.5 V

By applying Kirchoff's Laws to the fuel injection coil circuit we find

$$V_{DD} = L \times \frac{dI(t)}{dI} + R_L i(t) + V_{AV} \quad (9)$$

Using boundary condition at t = 0, i(t) = I_L = I_{AR}, yields the general solution in the time domain:

Solving for the avalanche pulsewidth (t_{av}) assuming i(t_{av}) = 0 gives

$$i(t) = I_{AR} e^{\left(-\frac{R_L}{L}t\right)} + \frac{V_{AV} - V_{DD}}{R_L}\left[e^{\left(-\frac{R_L}{L}t\right)} - 1\right] \quad (10)$$

$$t_{AV} = \frac{L}{R_L} \times \ln\left[1 + \frac{I_{AR} \times R_L}{V_{AV} - V_{DD}}\right] = \quad (11)$$

$$= \frac{5\ mH}{15\ \Omega} \times \ln\left[1 + \frac{0.966\ A \times 15\ \Omega}{52\ V - 14.5\ V}\right] = 109\ \mu s$$

since avalanche voltage can be obtained from measurement (best), or estimated from the 40 V/14 A MOSFET datasheet using equation 6 as

$V_{AV} \cong 1.3 \times BV_{DSS} = 1.3 \times 40\ V = 52\ V$

and avalanche current can be calculated as

Repetitive avalanche energy can be calculated as

APPLICATION NOTE

Power MOSFET Avalanche Design Guidelines

$$I_L = I_{AR} = \frac{V_{DD}}{R_L + R_{DS(on)}} = \frac{14.5\ V}{15\ \Omega + 10\ m\Omega} = 0.966\ A \quad (12)$$

$$E_{AR} = \frac{I_{AR} \times V_{AV} \times t_{AV}}{2} = \frac{0.966\ A \times 52\ V \times 109\ \mu s}{2} = 2.74\ mJ \quad (13)$$

Average avalanche, and conduction power values can be calculated as

$$P_{AV} = \frac{E_{AR}}{t_{AV}} = \frac{2.74\ mJ}{109\ \mu s} = 25.1\ W, \quad (14)$$

$$P_{ave} = E_{AR} \times f = 2.74\ mJ \times 125\ Hz = 343\ mW, \quad (15)$$

since the avalanche duty cycle can be calculated as

The average junction temperature can be calculated as

$$P_{cond.} = (I_L)^2 \times R_{DS(on)} \times D = (0.966\ A)^2 \times 10\ m\Omega \times 0.013 = 121\ \mu W \quad (16)$$

$$D = t_{AV} \times f = 109\ \mu s \times 125\ Hz = 0.013 \quad (17)$$

$$T_{SS} = (P_{ave} + P_{cond.}) \times R_\theta + T_A = (343\ mW + 121\ \mu W) \times 50\ °C/W + 120\ °C = 137.2\ °C \quad (18)$$

The peak rise in junction temperature due to each avalanche pulse is given by

$$\Delta T = P_{AV} \times Z_{TH} = 25.1\ W \times 0.18\ °C/W = 4.5\ °C \quad (19)$$

where the thermal impedance (Z_{TH}) is approximated from the transient thermal impedance plot provided with the datasheet, as shown in figure 23.

Note that $T_{SS} + \Delta T = 137.2\ °C + 4.5\ °C = 141.7\ °C < T_{J\ (max.)}$

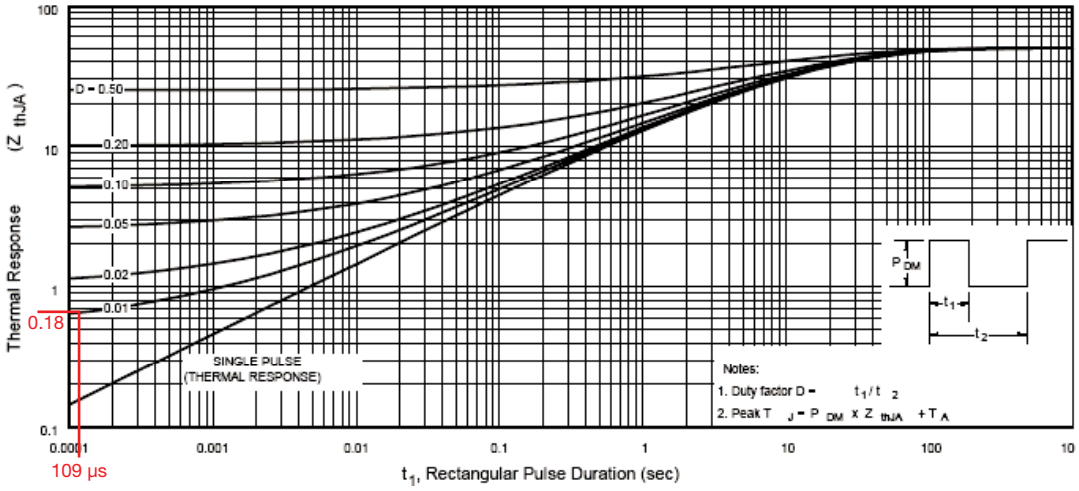

Fig. 23 - Typical Effective Transient Thermal Impedance, Junction-to-Ambient

BUYER BEWARE

Many suppliers rate power MOSFET avalanche capability with only a single number in the datasheet and without providing full circuit or test condition details. In such cases, buyer beware! It is not sufficient to merely compare the numeric values of avalanche energy which appear in datasheet tables. The following example will help illustrate one such pitfall.

Since avalanche energy depends on the inductor value and starting current, it is possible to have two pulses with the same energy but different shape provide two different junction temperatures. This phenomenon is illustrated in the following examples:

Example 1

Pulse:

$I_{AS} = 32\ A$
$L = 0.87\ mH$

Result:

$$E_{AS} = \frac{1}{2} \times L \times (I_{AS})^2 = 445\ mJ$$

$$t_{AV} = L \times \frac{I_{pk}}{V_{(AV)DSS}} \cong 43\ \mu s$$

$Z_{TH} = 0.012\ °C/W$
$\Delta T = 120\ °C$
$T_J = 145\ °C < T_{J\ (max.)}$

APPLICATION NOTE

Power MOSFET Avalanche Design Guidelines

Example 2

Pulse:

I_{AS} = 16 A
L = 3.48 mH

Result:

$$E_{AS} = \frac{1}{2} \times L \times (I_{AS})^2 = 445 \text{ mJ}$$

$$t_{AV} = L \times \frac{I_{pk}}{V_{(AV)DSS}} \cong 86 \text{ µs}$$

Z_{TH} = 0.02 °C/W
ΔT = 200 °C
T_J = 225 °C > $T_{J\ (max.)}$

Examples 1 and 2 both have the same energy, however, since the inductor varies, so does the junction temperature. While one junction temperature is within $T_{J\ (max.)}$, the second is not.

Note as well that power MOSFETs which are "E_{AS}" rated include graphs showing constant junction temperature energy values. See for example figure 20, top curve. Which value of energy should be compared with another suppliers power MOSFET?

Another common industry practice is to rate avalanche capability based on curves showing allowable time in avalanche as a trade-off with drain current. At best, such curves are backed up with test to failure data as seen in figure 10. However, sometimes these curves are based on statistically determined limits without apparent regard for junction temperature. The result is that a thermal T_J calculation (see examples 1 and 2) for the rated allowed condition may show that T_J exceeds $T_{J\ (max.)}$, without reliability qualification data at this higher than $T_{J\ (max.)}$ condition. Again, buyer beware.

CONCLUSION

Vishay applies 3 different classes of avalanche rating:

- The thermal approach allows single pulse and (where indicated) repetitive pulse avalanche operation as long as neither $I_{D\ (max.)}$ nor rated $T_{J\ (max.)}$ are exceeded. Energy losses due to avalanche operation can be analyzed as any other source of power dissipation. Such thermally rated parts are indicated by Vishay with a rating of "E_{AS}" and, more recently, with inclusion of repetitive avalanche SOA graph 9 (for example see figures 20 and 21).
- Statistically based avalanche ratings are set based on sample failure statistics. At this rating is labeled "E_{AS} (tested)" and corresponds to a production test screening limit. While the statistical approach generally gives higher energy value, it does not provide a practical method for evaluating avalanche capability in conditions that differ from the datasheet. Since circuit designers' conditions usually differ significantly, the statistical approach does not give a clear idea on how to design for occurrence of avalanche.
- Some legacy products were designed without an avalanche rating. Devices without an avalanche rating on the datasheet should not be used In circuits which will see avalanche condition during any mode of operation. By special arrangement, most such designs can be avalanche guaranteed; contact factory representative for further information.

Power MOSFET users should take care to understand differences in avalanche rating conditions between various suppliers. Devices that are not "avalanche robust" can cause unexpected and seemingly unexplained circuit failure. Some manufacturers do not rate their MOSFETs for avalanche at all. Others use a statistical rating alone which does not offer the same assurance for robust operation provided by a more complete characterization and rating.

APPLICATION NOTE