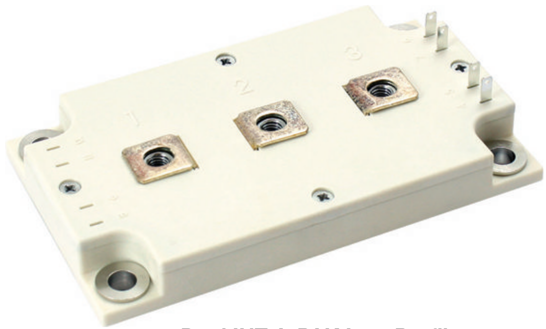
Dual INT-A-PAK Low Profile "Half Bridge" (Standard Speed IGBT), 400 A



Dual INT-A-PAK Low Profile

PRIMARY CHARACTERISTICS	
V_{CES}	600 V
I_C DC at T_C = 114 °C	400 A
$V_{CE(on)}$ (typical) at 400 A, 25 °C	1.14 V
Speed	DC to 1 kHz
Package	Dual INT-A-PAK low profile
Circuit configuration	Half bridge

FEATURES

- TrenchStop IGBT technology
- Standard: optimized for hard switching speed
- Low $V_{CE(on)}$
- Square RBSOA
- Gen 4 FRED Pt® dices technology
- Industry standard package
- Al_2O_3 DBC
- UL approved file E78996
- Designed for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS
COMPLIANT

BENEFITS

- Increased operating efficiency
- Performance optimized as output inverter stage for TIG welding machines
- Direct mounting on heatsink
- Very low junction to case thermal resistance

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MAX.**	**UNITS**
Collector to emitter voltage	V_{CES}		600	V
Continuous collector current	I_C (1)	T_C = 25 °C	711	A
		T_C = 80 °C	532	
Pulsed collector current	I_{CM}	T_C = 175 °C, t_p = 6 ms, V_{GE} = 15 V	1100	
Clamped inductive load current	I_{LM}		900	
Diode continuous forward current	I_F	T_C = 25 °C	260	
		T_C = 80 °C	192	
Gate to emitter voltage	V_{GE}		± 20	V
Maximum power dissipation (IGBT)	P_D	T_C = 25 °C	1364	W
		T_C = 80 °C	864	
Maximum power dissipation (Diode)	P_D	T_C = 25 °C	441	W
		T_C = 80 °C	279	
RMS isolation voltage	V_{ISOL}	Any terminal to case (V_{RMS} t = 1 s, T_J = 25 °C)	3500	V

Note

(1) Maximum continuous collector current must be limited to 500 A to do not exceed the maximum temperature of terminals

ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise specified)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Collector to emitter breakdown voltage	$V_{BR(CES)}$	V_{GE} = 0 V, I_C = 1.2 mA	600	-	-	V
Collector to emitter voltage	$V_{CE(on)}$	V_{GE} = 15 V, I_C = 400 A	-	1.14	1.40	
		V_{GE} = 15 V, I_C = 400 A, T_J = 125 °C	-	1.13	-	
Gate threshold voltage	$V_{GE(th)}$	V_{CE} = V_{GE}, I_C = 6 mA	3.8	4.7	6.3	
Collector to emitter leakage current	I_{CES}	V_{GE} = 0 V, V_{CE} = 600 V	-	0.002	0.3	mA
		V_{GE} = 0 V, V_{CE} = 600 V, T_J = 125 °C	-	1.1	-	
Diode forward voltage drop	V_{FM}	I_{FM} = 400 A	-	1.65	2.26	V
		I_{FM} = 400 A, T_J = 125 °C	-	1.58	-	
Gate to emitter leakage current	I_{GES}	V_{GE} = ± 20 V	-	-	± 200	nA

SWITCHING CHARACTERISTICS (T_J = 25 °C unless otherwise specified)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Total gate charge (turn-on)	Q_g	I_C = 75 A, V_{CC} = 520 V, V_{GE} = 15 V	-	2791	-	nC
Gate-to-emitter charge (turn-on)	Q_{ge}		-	428	-	
Gate-to-collector charge (turn-on)	Q_{gc}		-	711	-	
Turn-on switching loss	E_{on}	I_C = 400 A, V_{CC} = 300 V, V_{GE} = 15 V, R_g = 1.5 Ω, L = 500 μH, T_J = 25 °C	-	2.5	-	mJ
Turn-off switching loss	E_{off}		-	20.7	-	
Total switching loss	E_{tot}		-	23.2	-	
Turn-on switching loss	E_{on}	I_C = 400 A, V_{CC} = 300 V, V_{GE} = 15 V, R_g = 1.5 Ω, L = 500 μH, T_J = 125 °C	-	2.2	-	
Turn-off switching loss	E_{off}		-	27.6	-	
Total switching loss	E_{tot}		-	29.8	-	
Turn-on delay time	$t_{d(on)}$		-	24	-	ns
Rise time	t_r		-	104	-	
Turn-off delay time	$t_{d(off)}$		-	506	-	
Fall time	t_f		-	167	-	
Reverse bias safe operating area	RBSOA	T_J = 175 °C, I_C = 900 A, V_{CC} = 300 V, V_p = 600 V, R_g = 27 Ω, V_{GE} = 15 V to -5 V, L = 500 μH	Fullsquare			
Diode reverse recovery time	t_{rr}	I_F = 50 A, dI_F/dt = 500 A/μs, V_{CC} = 200 V, T_J = 25 °C	-	152	-	ns
Diode peak reverse current	I_{rr}		-	24	-	A
Diode recovery charge	Q_{rr}		-	1.82	-	μC
Diode reverse recovery time	t_{rr}	I_F = 50 A, dI_F/dt = 500 A/μs, V_{CC} = 200 V, T_J = 125 °C	-	200	-	ns
Diode peak reverse current	I_{rr}		-	39	-	A
Diode recovery charge	Q_{rr}		-	3.94	-	μC

THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER		**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Operating junction and storage temperature range		T_J, T_{Stg}	-40	-	175	°C
Junction to case per leg	IGBT	R_{thJC}	-	-	0.11	°C/W
	Diode		-	-	0.34	
Case to sink per module		R_{thCS}	-	0.05	-	
Mounting torque	case to heatsink: M6 screw		4	-	6	Nm
	case to terminal 1, 2, 3: M5 screw		2	-	5	
Weight			-	270	-	g

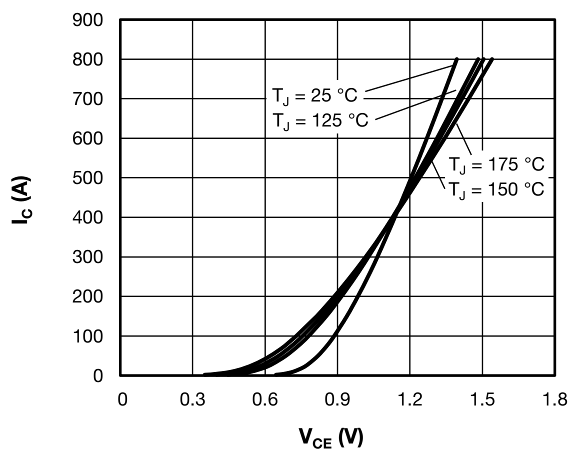


Fig. 1 - Typical Q1 to Q2 IGBT Output Characteristics, V_{GE} = 15 V

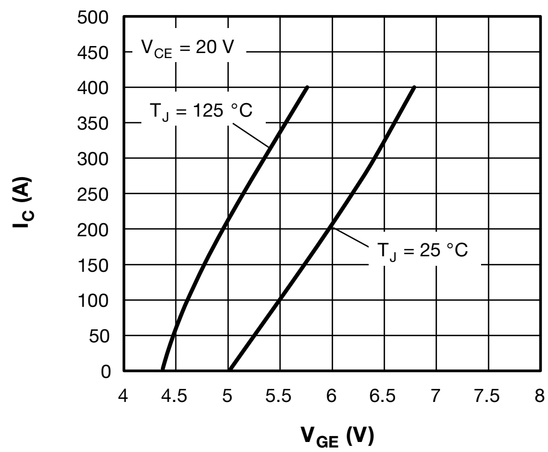


Fig. 4 - Typical Q1 to Q2 IGBT Transfer Characteristics

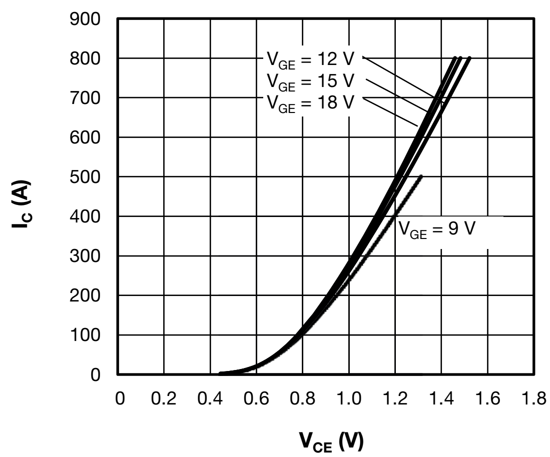


Fig. 2 - Typical Q1 to Q2 IGBT Output Characteristics, T_J = 125 °C

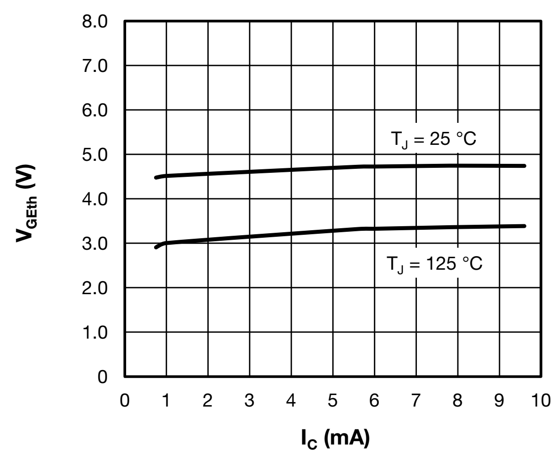


Fig. 5 - Typical Q1 to Q2 IGBT Gate Threshold Voltage

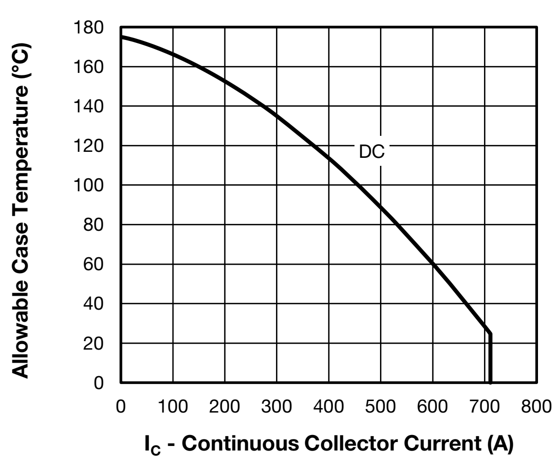


Fig. 3 - Maximum Q1 to Q2 IGBT Continuous Collector Current vs. Case Temperature

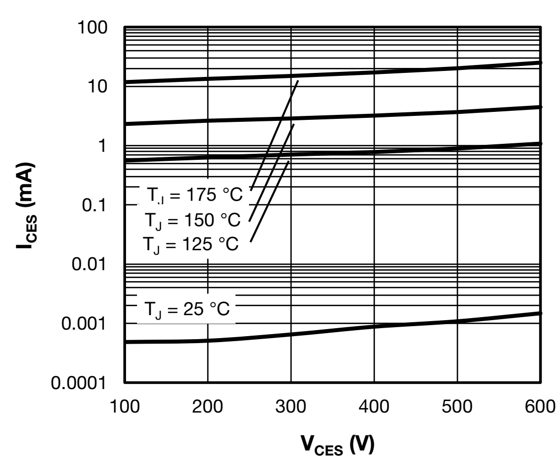


Fig. 6 - Typical Q1 to Q2 IGBT Zero Gate Voltage Collector Current

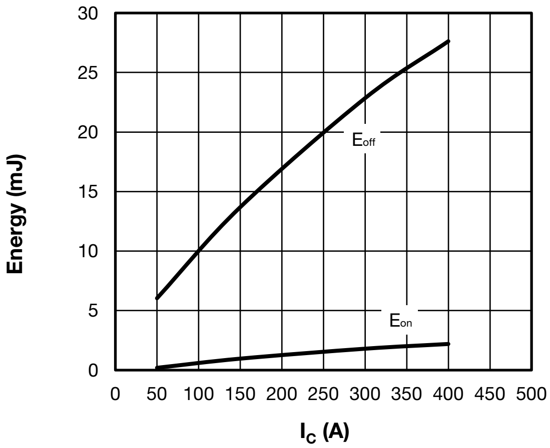


Fig. 7 - Typical Q1 to Q2 IGBT
Energy Loss vs. I_C (with D1 to D2 Antiparallel Diode)
T_J = 125 °C, V_{CC} = 300 V, R_g = 1.5 Ω, V_{GE} = +15 V /-15 V, L = 500 μH

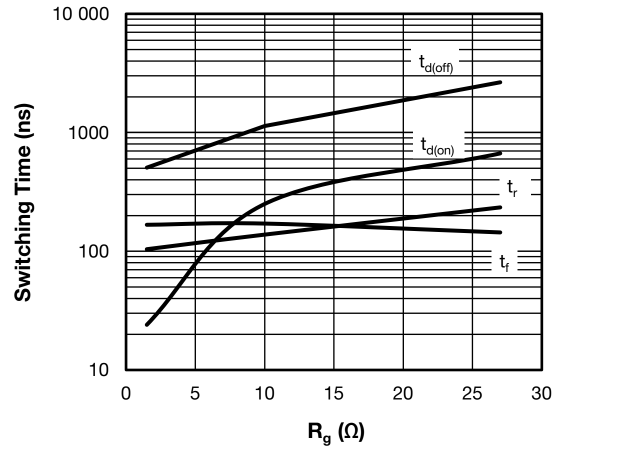


Fig. 10 - Typical Q1 to Q2 IGBT
Switching Time vs. R_g (with D1 to D2 Antiparallel Diode)
T_J = 125 °C, V_{CC} = 300 V, I_C = 400 A, V_{GE} = +15 V/-15 V, L = 500 μH

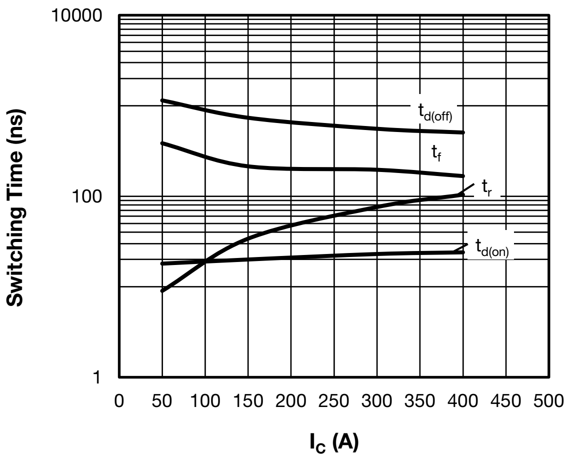


Fig. 8 - Typical Q1 to Q2 IGBT
Switching Time vs. I_C (with D1 to D2 Antiparallel Diode)
T_J = 125 °C, V_{CC} = 300 V, R_g = 1.5 Ω, V_{GE} = +15 V /-15 V, L = 500 μH

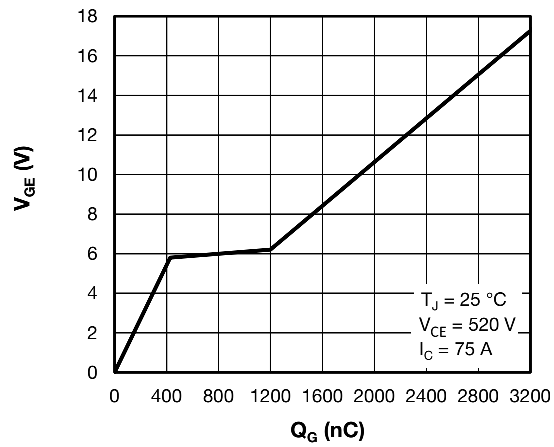


Fig. 11 - Typical Q1 to Q2 IGBT
Gate Charge vs. Gate to Emitter Voltage

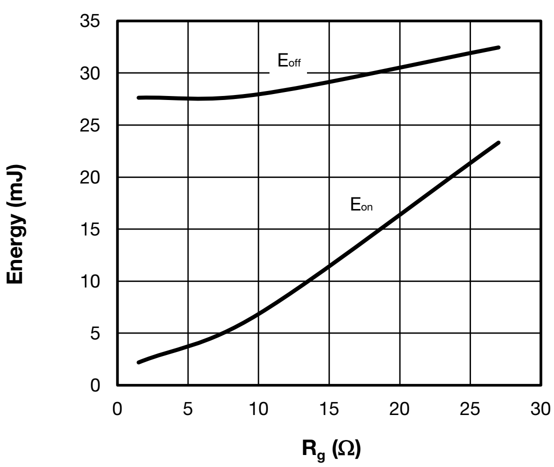


Fig. 9 - Typical Q1 to Q2 IGBT
Energy Loss vs. R_g (with D1 to D2 Antiparallel Diode)
T_J = 125 °C, V_{CC} = 300 V, I_C = 400 A, V_{GE} = +15 V/-15 V, L = 500 μH

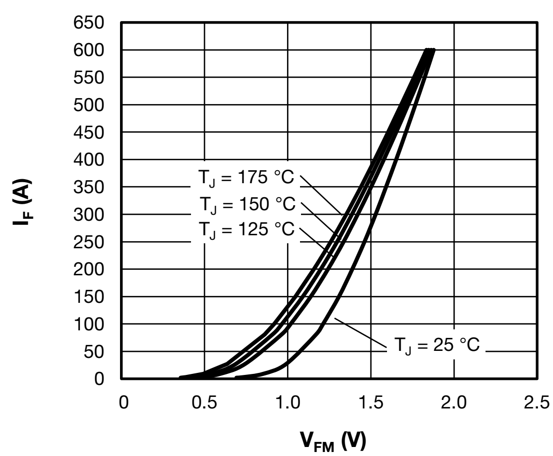


Fig. 12 - Typical D1 to D2 Antiparallel Diode
Forward Characteristics

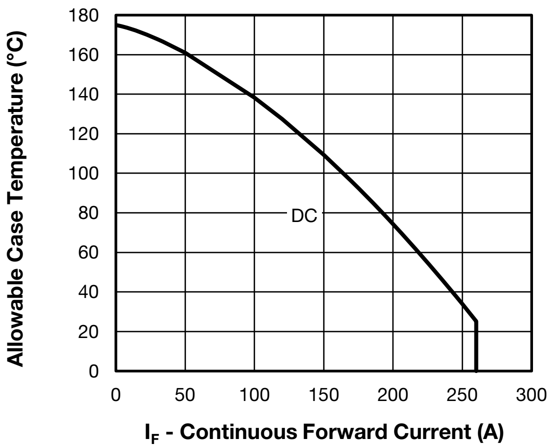


Fig. 13 - Maximum D1 to D2 Antiparallel Diode Continuous Forward Current vs. Case Temperature

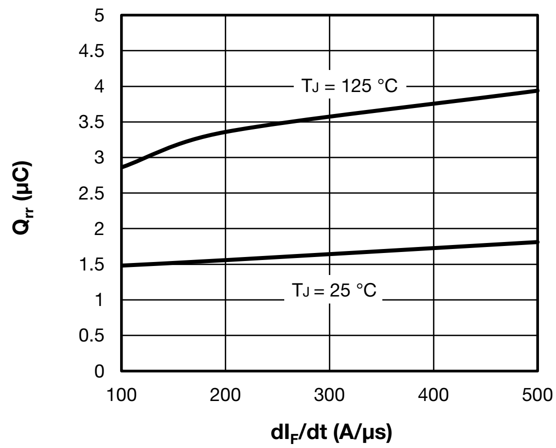


Fig. 16 - Typical D1 to D2 Antiparallel Diode Reverse Recovery Charge vs. dI_Fdt, V_{CC} = 200 V, I_F = 50 A

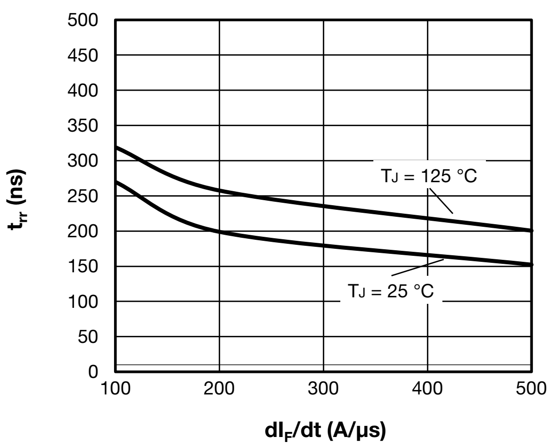


Fig. 14 - Typical D1 to D2 Antiparallel Diode Reverse Recovery Time vs. dI_Fdt
V_{CC} = 200 V, I_F = 50 A

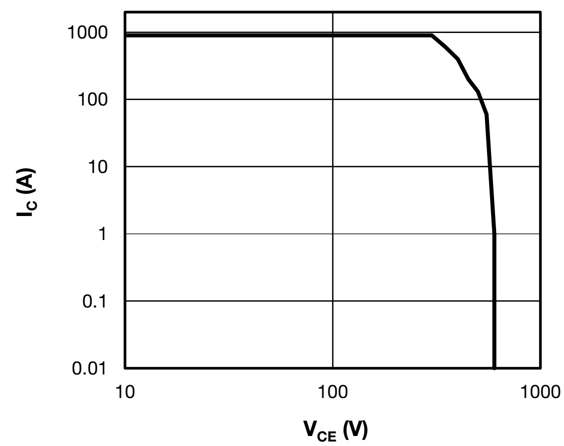


Fig. 17 - Q1 to Q2 IGBT Reverse BIAS SOA
T_J = 175 °C, I_C = 900 A, R_g = 27Ω, V_{GE} = +15 V / -5 V, V_{CC} = 300 V, V_p = 600 V

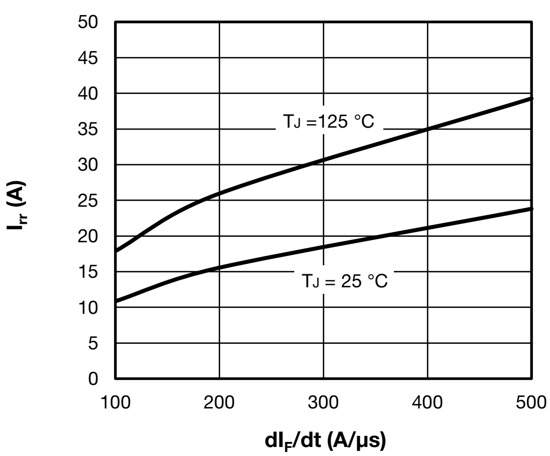


Fig. 15 - Typical D1 to D2 Antiparallel Diode Reverse Recovery Current vs. dI_Fdt, V_{CC} = 200 V, I_F = 50 A

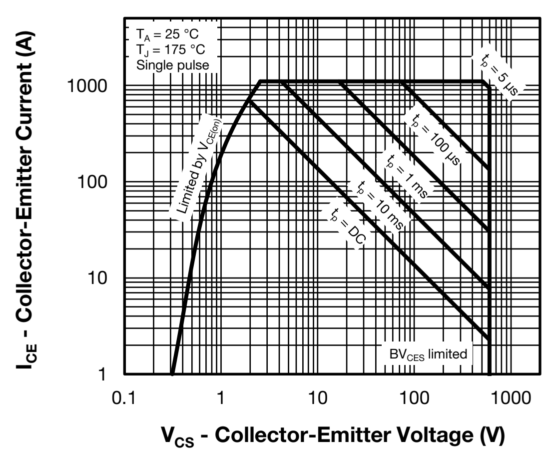


Fig. 18 - Q1 to Q2 IGBT Safe Operating Area

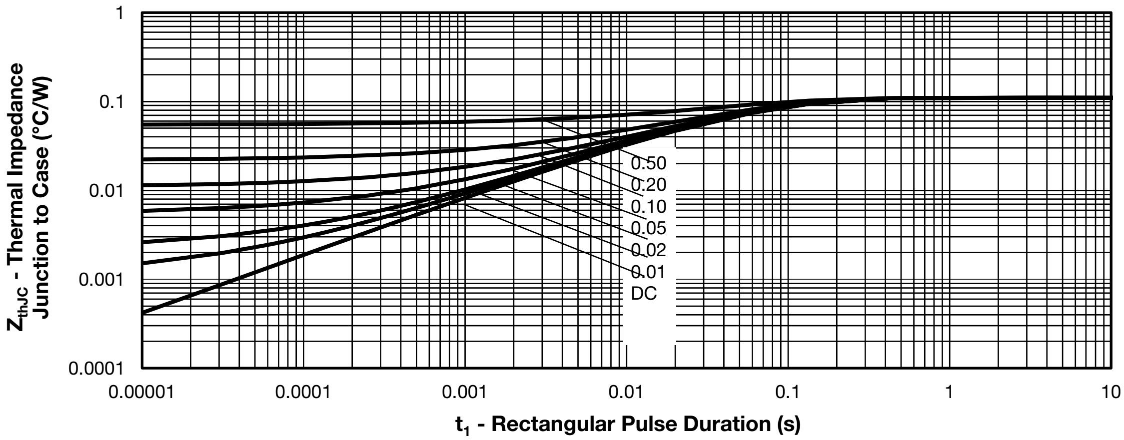


Fig. 19 - Maximum Thermal Impedance Z_{thJC} Characteristics - (Q1 to Q2 IGBT)

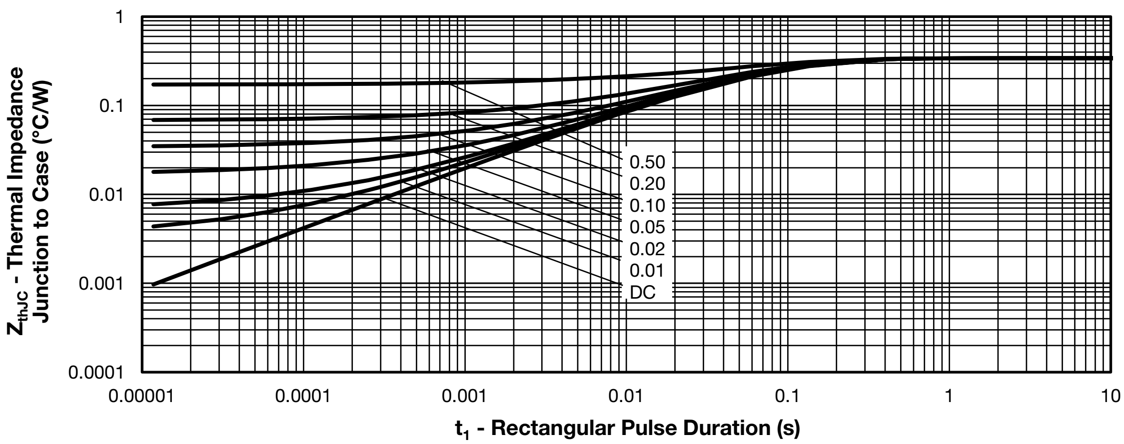


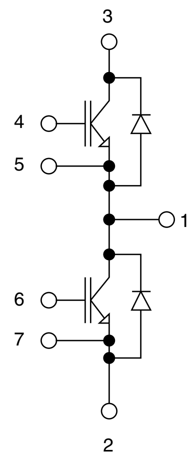
Fig. 20 - Maximum Thermal Impedance Z_{thJC} Characteristics - (D1 to D2 Antiparallel Diode)

ORDERING INFORMATION TABLE

Device code	G	T	400	T	D	60	S
	1	2	3	4	5	6	7

1	-	Insulated gate bipolar transistor (IGBT)
2	-	T = Trench IGBT technology
3	-	Current rating (400 = 400 A)
4	-	Circuit configuration (T = half-bridge)
5	-	Package indicator (D = dual INT-A-PAK low profile)
6	-	Voltage rating (60 = 600 V)
7	-	Speed / type (S = standard speed IGBT)

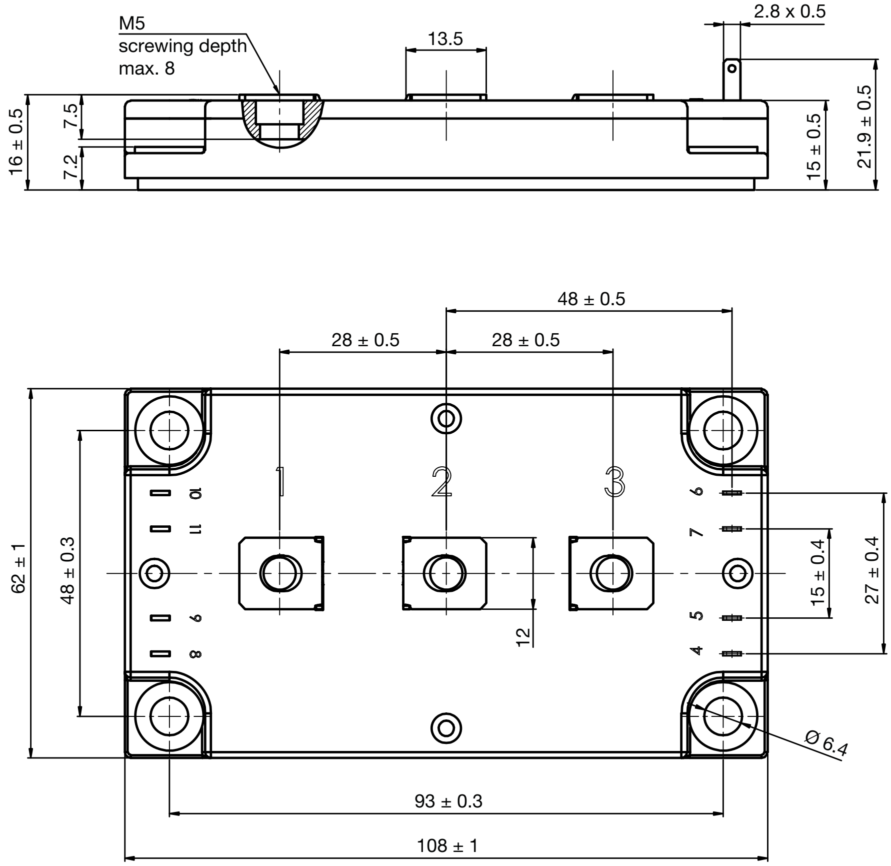
CIRCUIT CONFIGURATION



LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95435

Dual INT-A-PAK Low Profile

DIMENSIONS in millimeters



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